Performance Evaluation of the Input and Output Buffered Knockout Switch

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ABSTRACT

Various ATM switches have been proposed since Asynchronous Transfer Mode (ATM) was recognized as appropriate for implementing broadband integrated services digital network (B-ISDN). An ATM switching network may be evaluated on two sides : traffic performances (maximum throughput, delay, and packet loss probability, etc.) and structural features (complexity, i.e. the number of switch elements necessary to construct the same size switching network, maintenance, modularity, and fault tolerance, etc.). ATM switching networks proposed to date tend to show the contrary characteristics between structural features and traffic performance. The Knockout Switch, which is well known as one of ATM switches, shows a good traffic performance but it needs so many switch elements and buffers.

In this paper, we propose an input and output buffered Knockout Switch for the purpose of reducing the number of switch elements and buffers of the existing Knockout Switch. We analyze the traffic performance and the structural features of the proposed switching architecture through a discrete time Markov chain and compare with those of the existing Knockout Switch. It was found that the proposed architecture could reduce more than 40 percent of switch elements and more than 30 percent of buffers under a given requirement of cell loss probability of the switch.

1. Introduction

Since Asynchronous Transfer Mode (ATM) switching technology was recognized to be appropriate for implementing B-ISDN which should provide high switching speed and flexibility for various services, a variety of ATM switching architectures have been proposed [1, 3, 4, 5, 6, 9, 10, 11, 12,

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13, 14]. ATM switches proposed to date can be classified in two criteria : 1) input buffering and output buffering on the basis of resolution of output contention, and 2) single stage and multistage, based on the implementing method of switch module for composing the entire switching network[15].

An ATM switching network may be evaluated on two sides : traffic performances (maximum throughput, delay, and packet loss probability, etc.) and structural features (complexity, i.e. the number of switch elements necessary to construct the same size switching network, maintenance, modularity, and fault tolerance, etc.). Each switching group classified above tends to show the contrary characteristics between structural features and traffic performance.

Input buffering simplifies buffer structure [6, 10] but it allows head-of-line (HOL) blocking, which degrades maximum throughput as compared with output buffering [2, 7]. On the other hand, output buffering is superior in traffic performances such as maximum throughput and delay. However, it requires a special method of increasing line speed of the switch [3, 5, 9, 12] or more hardwares [1, 14] so that all output ports could be accessed from all input ports. Regarding the second classification, single-stage switch needs much more hardware devices than multi-stage switch does, while it can decrease delay within the switch and is easier of modular growth and maintenance, etc. On the other hand, multi-stage switch has a merit of embodying switch module by smallest switch elements, but it may cause congestion (i.e. blocking) at each switch element. This problem requires a special scheme [4, 13], which causes switch fabric to be complex and hence increases delay within the switch.

The Knockout Switch proposed by *Yeh et al.* [14], as is well known as one of ATM switches, is structured by single-stage and output buffering method. Figure.1 and Figure.2 show the interconnection fabric of the Knockout Switch and the bus interface with N : L concentrator, respectively. Since the Knockout Switch adopts output buffering method as shown in Figure.2, it seems to be good in traffic performance. On the other hand, as it is structured by single-stage, it is good in structural features. However, the major dismerit is that it needs so many switch elements and buffers. As shown in Figure.1, each input has a direct path to every output, and so no blocking occurs in the switch. On the other hand, packets destined for the same output can arrive simultaneously on the bus interface, which causes the output contention and results in packet loss. In order to decrease this loss probability, the Knockout Switch is designed to receive simultaneously up to L packets at the concentrator of bus interface as shown in Figure.2. This creates the major source of complexity in the switch. For a concentrator with N inputs and L outpus, about LN 2x2 switch elements and L buffers are needed[14] and therefore a total of LN^2 ($N \gg L$) 2x2 switch elements and LN buffers are needed. Hence, extremely large number of switch elements and buffers will be needed as the switch size grows.

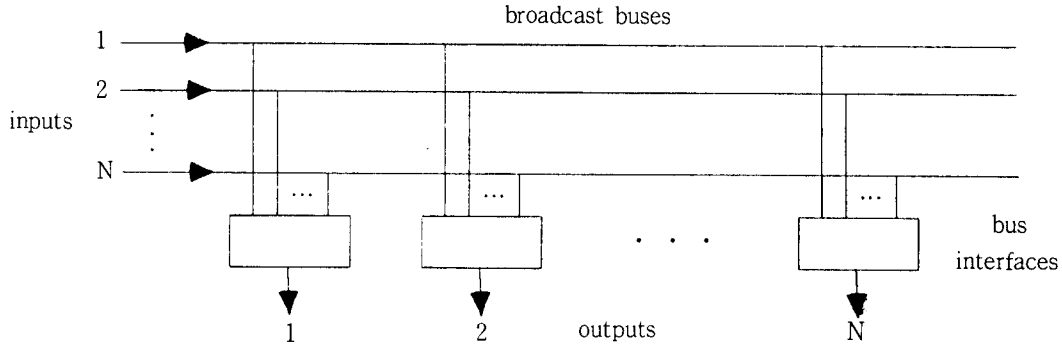

Figure 1. Interconnection Fabric of the Knockout Switch[14]

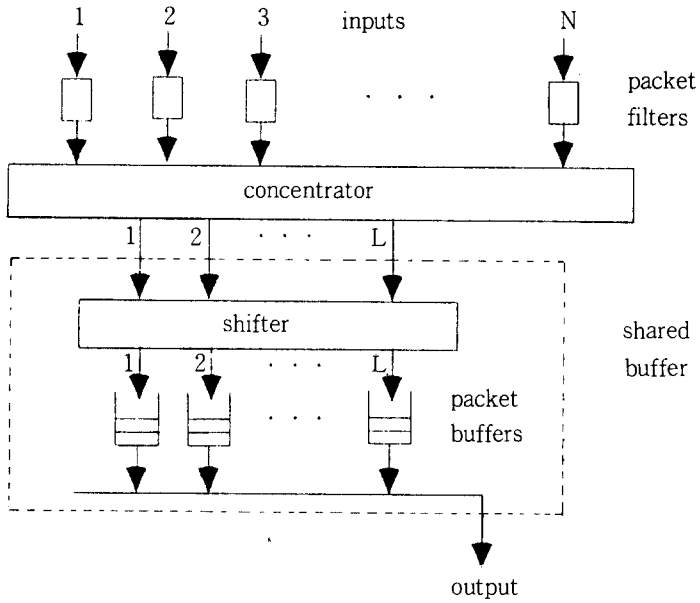

Figure 2. Bus Interface[14]

This paper focuses on reducing the complexity of the Knockout Switch, i.e. the number of switch elements and buffers, without degrading the traffic performance of the switch. Intuitively, we can consider an alternative of decreasing L, the number of concentrator output. If we can decrease L by only one, a total of N^2 switch elements and N buffers can be reduced. But if L is decreased, then packet loss probability at concentrator may be increased and loss requirement within the switch cannot be met at high input load. Here, we must consider a way to compensate the increase of loss probability at concentrator. Employing input buffer at each input port of the switch can be one solution. In order words, we can avoid losing packets at concentrator by storing

the packets dropped at the concentrator in their corresponding input buffers. But input buffer may accompany several performance problems.

Following introduction, we describe the switching architecture of the input and output buffered Knockout Switch and input buffer-related performance problems in Sec.2. In Sec.3, we analyze the traffic performance measures such as packet loss probability, maximum throughput and delay and the complexity of the input and output buffered Knockout Switch, and compare with those of the existing Knockout Switch. Finally, we discuss the result and state the conclusions in Sec.4.

2. Input and Output Buffered Knockout Switch

2.1 Description of the Input and Output Buffered Knockout Switch

For convenience, let us call the existing Knockout Switch the KS and the input and output buffered Knockout Switch the IOBKS. Like the KS, the IOBKS is a packet switch with all inputs and outputs operating at the same bit rate. As shown in Figure.3, the interconnection fabric of the IOBKS is similar to that of the KS. That is, each input has a separate broadcast bus and a buffer, and each output has access to the cells arriving at all inputs. The only difference from the KS is that each input has a buffer.

Fixed-length packets, called *cells*, arrive at input buffers and depart from them in a time slotted-fashion. Each cell contains the address of the output port for which it is destined. All arriving cells wait at their input buffers until they reach the head-of-line (HOL) positions. When a cell is at the HOL position, it may compete with other cells destined for the same output port in the time slot in order to be transferred. The competition is made at concentrator with limited outputs. Only the cells which win the competition are transferred to their corresponding output (shared) buffers and the others remain at the HOL position until they are eventually transferred. This process can be accomplished as following : i) copy the head of each cell to be transferred which contains the destination address, ii) send it to the corresponding concentrator for competition, iii-a) if it wins the competition, return an acknowledgement message along the opened way through which the headd is passed and then iv-a) transfer the whole information of the acknowledged cell. iii-b) otherwise, let the non-acknowledged cell remain as it is. Therefore, cell loss does not happen at concentrator.

The bus interface (associated with an output) is structured just like for the KS as shown in Figure.2. That is, the bus interface has three major components : N packet filters, an N-to-L concentrator and a shared buffer. The functions of these components are described below. The details for the bus interface may refer to[14].

Packet Filters : The address of every arriving cell is examined here by bit-by-bit comparison. If the address of an arriving cell is different from the corresponding output, that cell is blocked. Only the cell with the same address as the output is allowed to pass on the concentrator.

Concentrator : Achieving an N to L concentration of the inputs, a concentrator selects up to L cells among the cells passed through the packet filters and sends them to its shared buffer. If more than L cells are destined for this bus interface in a given time slot, the only L cells are selected at the concentrator and the rest must wait for the next chance (i.e. the next time slot) in their input buffers. More detailed description will be made in the next section.

Shared Buffer : A shared buffer is composed of a shifter and L separate FIFO buffers. A shifter has L inputs and L outputs, shifting circularly inputs to outputs so that the L separate buffers are filled in a cyclic fashion. Since cells are stored in and removed from the L buffers in a cyclic fashion, the shared buffer allows complete sharing of the L FIFO buffers and provides the equivalent of a single queue with L inputs and one output, operating under a first-in first-out queueing discipline.

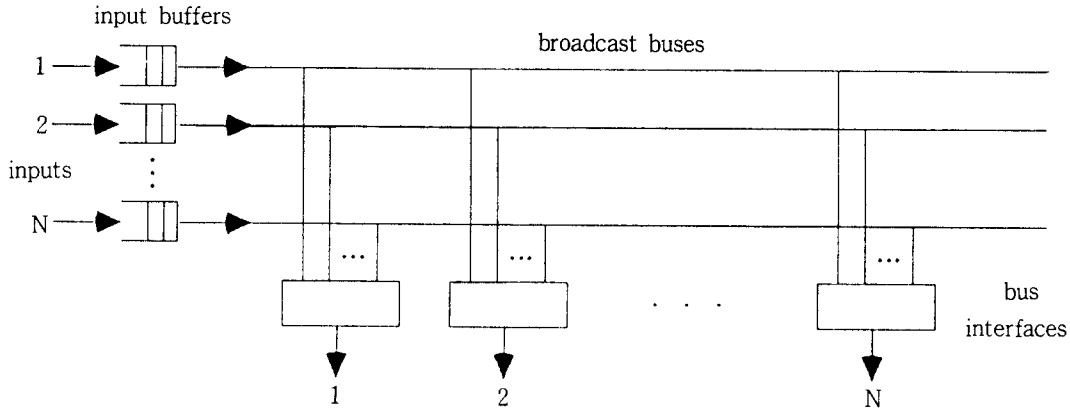

Figure 3. The Interconnection Fabric of the IOBKS

2.2 Input Buffer-Related Performance Problems

The following performance problems should be considered in the IOBKS.

1) Cell loss probability

While cell loss due to congestion at the concentrator is avoidable in the IOBKS, cell loss may result from input buffer overflow. The cell loss due to input buffer must be compared with loss in the KS and it should meet the requirement of loss probability. And the cell loss probability at

shared buffer should not be degraded by decreasing the number of its separate buffers which results from reducing the number of concentrator outputs.

2) Maximum throughput

Input buffering allows the HOL blocking, which may degrade maximum throughput of the switch.

3) Delay

The HOL blocking due to input buffer may increase delay within the switch. This increased fraction of delay should be small enough to have little impact on the performacne of the switch.

In the next section, the input buffer-related performance problems of the IOBKS mentioned above will be analyzed and performance measures are compared with those of the KS.

3. Performance Evaluation of the IOBKS

The IOBKS aims at reducing the complexity of the switch by decreasing the number of conentrator outputs and employing input buffers. First of all, therefore, we analyze the cell loss at the concentrator in case of the KS and the loss at the input buffer in case of the IOBKS, and compare with each other. Then, we investigate how much the complexity of the IOBKS could be reduced as compared with that of the KS for the same loss requirement. Other performance measures of the IOBKS are also evaluated.

3.1 Cell Loss Probability

The IOBKS has two sources of cell loss as the KS does. First, cell loss takes place by the congestion at concentrator in the KS, whereas it takes place by overflow of input buffer in the IOBKS. Second, cell loss takes place by overflow of shared buffer in both the KS and the IOBKS.

1) Loss Probability at Concentrator or Input Buffer

Loss Probability at the Concentrator of the KS

Assume that traffic is equally distributed on both input and output sides of the switch and that in a time slot a cell arrives at each input port independently of others with probability α. These assumptions will be applied through the paper. Then, the probability of n cells arriving at N inputs in a time slot, $q_{N,n}$, has the binomial probabilites

$$q_{N,n} = {}_NC_n\, \alpha^n\, (1-\alpha)^{N-n}, \quad n=0, 1, \cdots, N. \tag{1}$$

Let $P_{n,k}$ be the probability that among n arriving cells k cells are destined for a given output of the switch. Then it also has the binomial probabilities

$$P_{n,k} = {}_nC_k (1/N)^k (1-1/N)^{n-k}, \quad k=0, 1, \cdots, n. \tag{2}$$

Since we are concerned with the complexity of the switch (i.e. the number of switch elements and buffers), a large-scaled switch is considered. For large N, therefore, the limiting probability that k cells are destined for a given output of the switch reduces to the Poisson probabilities with mean α, which is same as the input load on the switch.

$$P_k = \lim_{N\to\infty} \sum_{n=k}^{N} q_{N,n} P_{n,k} = \lim_{N\to\infty} \binom{N}{k} \left(\frac{\alpha}{N}\right)^k \left(1-\frac{\alpha}{N}\right)^{N-k} = \frac{e^{-\alpha}\alpha^k}{k!}, \quad k=0, 1, \cdots \tag{3}$$

The KS is designed to receive simultaneously up to L cells at a concentrator with L outputs as shown in Figure.2. Thus, if more than L cells arrive at a concentrator, cell loss takes place. Let μ be the average number of cells passed through a concentrator in a time slot, then it is same for all the concentrators and is given by

$$\mu = \sum_{k=1}^{L} kP_k + L\sum_{k=L+1}^{\infty} P_k = L - \sum_{k=0}^{L} P_k (L-k). \tag{4}$$

Since the average number of cells arriving at a concentrator in a time slot is α, the limiting probability of a cell being dropped (i.e. lost) in the concentrator, β, can be derived by

$$\beta = (\alpha-\mu)/\alpha = 1-\frac{L}{\alpha} + \frac{1}{\alpha}\sum_{k=0}^{L} \frac{e^{-\alpha}\alpha^k}{k!} (L-k). \tag{5}$$

For $N\to\infty$, Figure.4 shows the loss probability versus the number of concentrator outputs for the various input load α. As shown in Figure.4, if the input load of the switch is more than 70 percent, the KS needs more than 8 concentrator outputs for the loss requirement of 10^{-6}. Table 1 shows the number of concentrator oututs of the KS needed for various input loads and loss requirements.

Loss Probability at the Input Buffer of the IOBKS

There is no cell loss at the concentrator of the IOBKS, since cells dropped at the concentrator will remain in their input buffers. Instead, cell loss may occur at input buffer. Each input buffer of the IOBKS can be considered as a single queue with finite capacity, operating under first-in first-out queueing discipline. Since a cell arrives at the corresponding input buffer with probability α each time slot independently of others, the cell interarrival time is geometrically distributed with parameter α. Similarly, since the service begins for a cell in the HOL position at the start of a time slot, the service time of a cell, the time until the cell actually leaves the buffer, is also

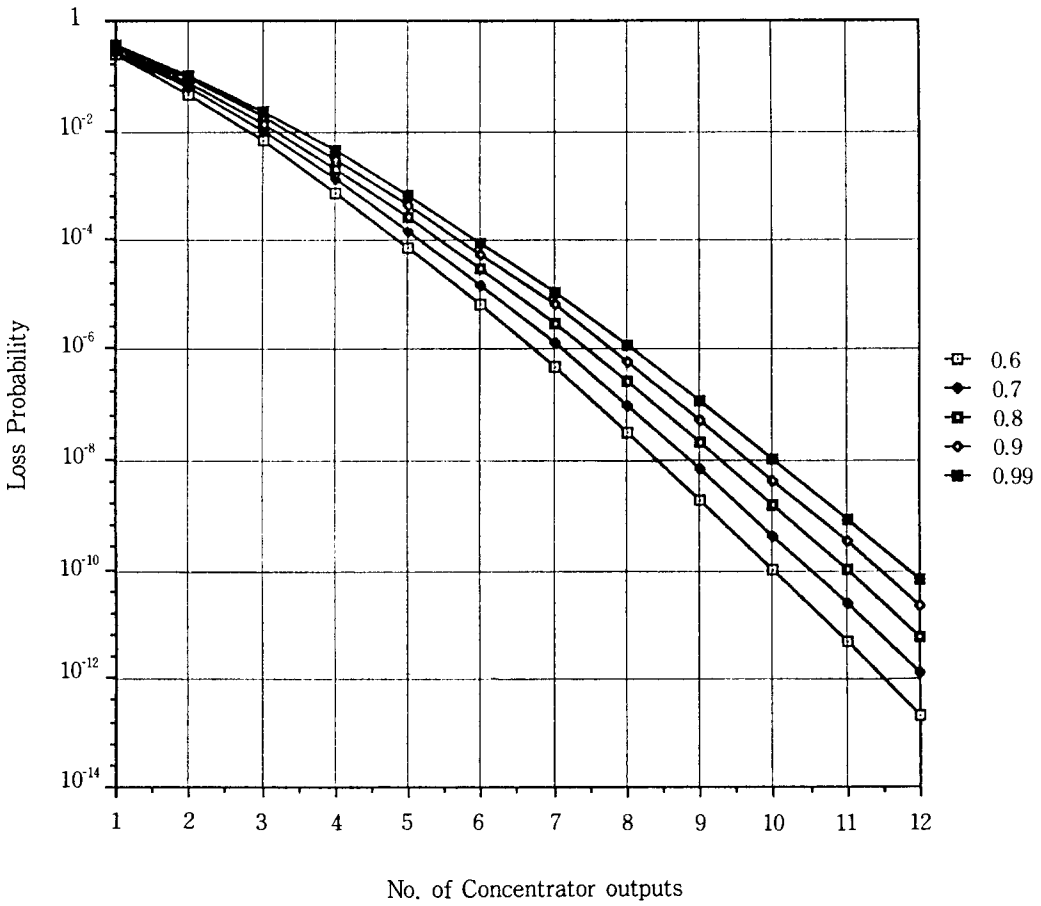

Figure 4. Loss Probability at Concentrator of the KS for the Various Input Load

Table 1. Number of Concentrator Outputs Required in the KS

α \ R	10^{-4}	10^{-8}	10^{-10}
0.6	7	9	10
0.7	8	9	11
0.8	8	10	11
0.9	8	10	12
0.99	9	11	12

α : inputs load on the switch

R : loss requirement

geometrically distributed with parameter $(1-\beta)$, where β is the probability of a cell being rejected at the concentrator. Therefore, the input buffer of the IOBKS can be modeled by a discrete-time Markov chain. Let us call the state of the Markov chain state i if the number of cells of input buffer at the end of a time slot equals i. Let s be the input buffer size. Suppose a cell arrives, if ever, at input buffer at the start of a time slot and departs from that at the end of a time slot. Because only one cell may arrive at and depart from the input buffer in a time slot, the state transition in a time slot takes place between neighboring states or themselves as shown in Figure 5. and the transition probability from state i to state j, P(i,j), in a time slot is as follows :

i) For i=0,

$$P(0,0) = \Pr\{\text{no arrival, or one arrival and one departure}\} = 1-\alpha\beta$$

$$P(0,1) = \Pr\{\text{one arrival and no departure}\} = \alpha\beta$$

ii) For i=1, 2, ···, s-1,

$$P(i,i+1) = \Pr\{\text{one arrival and no departure}\} = \alpha\beta$$

$$P(i,i-1) = \Pr\{\text{no arrival and one departure}\} = (1-\alpha)(1-\beta)$$

$$P(i,i) = \Pr\{\text{no arrival and no departure, or one arrival and one departure}\} = (1-\alpha)\beta+\alpha(1-\beta)$$

iii) For i=s,

$$P(s,s) = \Pr\{\text{no departure}\} = \beta$$

$$P(s,s-1) = \Pr\{\text{one departure}\} = 1-\beta$$

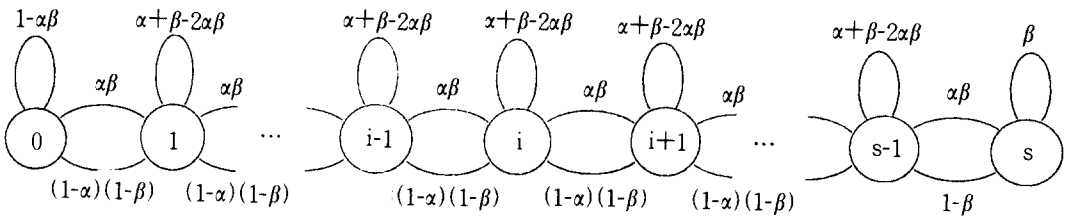

Figure 5. Discrete-Time Markov Chain for Input Buffer

Let Π and $\mathbf{P}$ denote the limiting probability vector and the transition probability matrix, respectively. Then, the limiting probabilities can be derived from $\Pi=\Pi\mathbf{P}$ and $\sum_{i=0}^{s}\Pi_i=1$ [8].

$$\Pi_i = \begin{cases} \rho^i\,\Pi_0, & \text{if } i\le s-1 \\ \rho^s\,(1-\alpha)\,\Pi_0, & \text{if } i=s \end{cases} \tag{6}$$

where

$$\Pi_0 = \left[\sum_{i=0}^{s}\rho^i - \alpha\rho^s\right]^{-1} \quad \text{and} \quad \rho = \frac{\alpha\beta}{(1-\alpha)(1-\beta)}\ .$$

To assess β, let us consider P_k, the probability that k cells are destined for a given output (i.e. concentrator) in the IOBKS. Recall that in the KS P_k has the Poisson probability with mean α. In the IOBKS, however, the average number of cells arriving at concentrator is not α any more since a cell can enter a concentrator if cells remain at input buffer even in the case of no arrival in the time slot. Therefore, the probability that in a time slot there exists at least one cell in a given input buffer to be delivered, α_1, is expressed by

$$\alpha_1 = \alpha+(1-\alpha)(1-\Pi_0) \tag{7}$$

That is, α_1 represents the average number of cells arriving at a given concentrator of the IOBKS. Strictly speaking, α_1 is dependent on input buffers, but the dependency may fade out for a large-scaled switch. In such a case, we can derive that P_k in the IOBKS has also the Possion probability with mean α_1 in the same manner as for the KS, and therefore the probability β of a cell being rejected at the concentrator of the IOBKS can be calculated from equation(5) using α_1 instead of α.

Since a cell will be lost if it arrives when input buffer is full at the end of the previous time slot, the cell loss probability by overflow of input buffer, γ, is given by

$$\begin{aligned}\gamma &= \alpha\,\Pi_s \\ &= \alpha(1-\alpha)\left(\frac{\alpha\beta}{(1-\alpha)(1-\beta)}\right)^s\Pi_0\end{aligned} \tag{8}$$

Figure. 6 shows, for α=0.9 (i.e., a 90 percent load), a plot of cell loss probability at input buffer as a function of s when L=4 and 5. As shown in Figure. 6, with input buffer being five deep, only four and five concentrator outputs of the IOBKS could, respectively, meet the requirements

of cell loss probabilities 10^{-6} and 10^{-10}, which would be satisfied with eight and twelve concentrator outputs in the KS. These result in reducing 50 percent and 58.3 percent of switch elements and 37.5 percent and 50 percent of buffers, respectively, as compared with the KS.

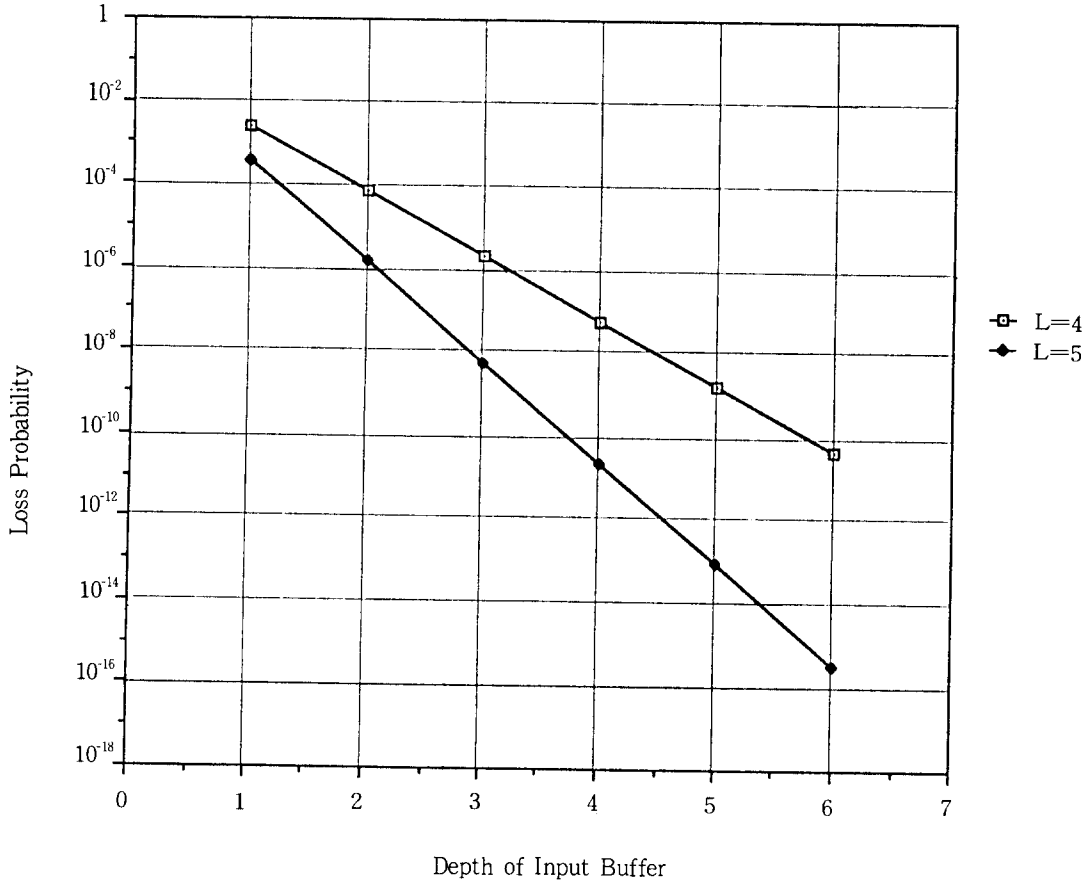

Figure 6. Loss Probability at Input Buffer of the IOBKS

Table 2. (a) and (b) show the number of concentrator outputs required (L_2) and the corresponding buffer size in the IOBKS (s) together with the number of concentrator outputs required in the KS (L_1) such that the specified requirement of cell loss probability should be met. As shown in Table 2, with each input buffer of the IOBKS being only five deep, the concentrator outputs of the IOBKS are needed less than half of those of the KS in all cases except for α=0.99 when the loss requirement is 10^{-6}. This means that the IOBKS can save more than 50 percent of switch elements and more than 30 percent of buffers. In the case of α=0.99 at loss requirement 10^{-6}, the IOBKS can save about 44 percent of switch elements and 33 percent of buffers. In addition, Table

2 shows that the more the requirement of loss probability is severe, the more savings of switch elements and buffers will be made.

Table 2. Required Number of Concentrator Outputs of the IOBKS

(a) loss requirement=10^{-6}

α	L_1	L_2	s
0.6	7	3	3
0.7	8	3	4
0.8	8	3	5
0.9	8	4	4
0.99	9	5	5

(b) loss requirement=10^{-10}

α	L_1	L_2	s
0.6	10	3	5
0.7	11	4	4
0.8	11	4	5
0.9	12	5	5
0.99	12	6	5

α : input load on the switch

L_1 : required no. of concentrator outputs of the KS

L_2 : required no. of concentrator outputs of the IOBKS

s : required input buffer size corresponding to L_2

2) Loss probability at Shared Buffer

The architecture of the shared buffer of the IOBKS is identical to that of the KS as shown in Figure. 2. That is, a shared buffer is composed of a shifter and L separate FIFO buffers, where L is determined by the number of concentrator outputs for meeting the loss requirement at input buffer in the IOBKS. As described in Sec. 2.1., since the shared buffer allows complete sharing of the L FIFO buffers, it can be expressed as a single queue with L combined inputs and one output (see Figure.8).

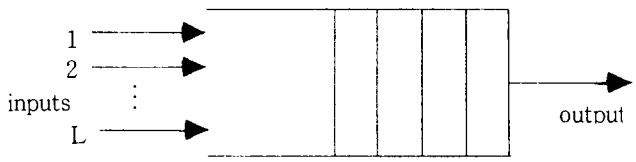

Figure 7. Shared Buffer

The total queue capacity of each shared buffer for the KS and the IOBKS can be determined to be equal to each other by adjusting the depth of separate buffers. Hence, the performance of the KS and the IOBKS about loss probability at the shared buffer can be compared indirectly by examing the average number of cells arriving at shared buffer in a time slot. Let L_1 and L_2 denote the number of concentrator of the KS and the IOBKS for meeting the loss requirement at concentrator of the KS and at input buffer of the IOBKS, respectively, for a given input load on the switch. Since a cell will arrive at the shared buffer when it passes the concentrator, the average number of cells arriving at the shared buffer in a time slot, $\bar{\lambda}$, is expressed by

$$\bar{\lambda} = \begin{cases} L_1 - \sum_{k=0}^{L_1} \frac{e^{-\alpha}\alpha^k}{k!}(L_1 - k), & \text{for the KS} \\ L_2 - \sum_{k=0}^{L_2} \frac{e^{-\alpha_1}\alpha_1^k}{k!}(L_2 - k), & \text{for the IOBKS} \end{cases} \quad (9)$$

where α represents the input load on the switch and α_1 is given in equation(7).

Table 3 shows the average number of cells arriving at each shared buffer in a time slot for various input loads and the corresponding L_1 and L_2 which meet the loss requirement 10^{-10}. We assume that the input buffer of the IOBKS is five deep in all cases. As shown in Table 3, the average number of cells arriving at the shared buffer of the IOBKS is almost the same as that of the KS. This result can be expected in advance, for it is calculated for the same requirement of loss probability at the concentrator of the KS and at the input buffer of the IOBKS, respectively. Hence, we can expect that the loss probability at each shared buffer of the KS and the IOBKS is almost the same for the equal total queue capacity and conclude that the IOBKS will not degrade the loss performance of the shared buffer. Yeh, et al.[14] modeled the shared buffer as an M/D/1 queue, assuming that all arriving cells enter the shared buffer for making the conservative approximation, and analyzed that with eight buffers, five cells deep each (a total of forty cells), the loss probability at the shared buffer of the KS is less than 10^{-6} for an 84 percent load on the switch. In the same manner, we will be able to derive the similar result with four buffers, ten cells deep each.

Table 3. The Average Number of Cells Arriving at Shared Buffer

(loss requirement : 10^{-10})

α	KS		α_1	IOBKS	
	L_1	$\bar{\lambda}$		L_2	$\bar{\lambda}$
0.6	10	0.5999	0.6039	3	0.5999
0.7	11	0.6999	0.7009	4	0.4999
0.8	11	0.7999	0.8016	4	0.7999
0.9	12	0.8999	0.9004	5	0.9000
0.99	12	0.9899	0.9909	6	0.9900

3.2 Maximum Throughput

The Maximum Throughput of the KS

The (normalized) maximum throughput of the KS is defined as the maximum input throughput of the shared buffer when the maximum output throughput of the shared buffer is considered as one. For infinite buffer size, the maximum input throughput of the shared buffer is $1 - \beta$ when the input load α on the switch is one, where β is the loss probability at the concentrator. Since β is extremely small for the number of concentrator outputs meeting the usual loss requirement, the maximum throughput of the KS is nearly one.

The Maximum Throughput of the IOBKS

For the purpose of obtaining the maximum throughput of the IOBKS, we assume that the input buffer size is infinite. Then, the limiting probabilities of input buffer states can be derived in the same manner as described in Sec. 3.1.

$$\Pi_i = \rho^i \Pi_0, \quad i=0, 1,\cdots \tag{10}$$

where

$$\Pi_0 = 1 - \rho \text{ and } \rho = \frac{\alpha\beta}{(1-\alpha)(1-\beta)}.$$

In above equation (10), α and β represent the input load on the switch and the probability of being rejected at concentrator, respectively. β is calculated by equation (5) using α_1 instead of α, where α_1 is given in equation(7).

The maximum throughput of the IOBKS can be defined as the minimum of the maximum input throughput of input buffer (that is, the maximum input load on the switch) and the maximum output throughput of input buffer, since the maximum output throughput of output (shared) buffer is one for infinite buffer size. For the purpose of input queueing system being stable, ρ must be less than one. Hence, the maximum throughput of the IOBKS, denoted by λ_{max}, is the maximum input load on the switch meeting the stable condition of the system and can be obtained by the solution to the following problem :

$$\begin{aligned} &\lambda_{max} = \max.\ \alpha \\ &\text{s.t.} \quad \frac{\alpha\beta}{(1-\alpha)(1-\beta)} < 1 \\ &\qquad \beta = 1 - \frac{L}{\alpha_1} + \frac{1}{\alpha_1} \sum_{k=0}^{L} \frac{e^{-\alpha_1} \alpha_1^k}{k!} (L-k) \\ &\qquad \alpha_1 = \frac{\alpha}{1-\beta} \qquad 0<\alpha,\ \beta,\ \alpha_1<1 \end{aligned} \tag{11}$$

In the above problem, λ_{max} can be computed iteratively by increasing the input load on the switch whose value could meet the given conditions. Table 4 shows the maximum throughput of the IOBKS for the various numbers of concentrator outputs. Note that λ_{max} grows quite rapidly as L increases, and that a maximum throughput of more than 99 percent can be achieved with L=4. In addition, there is little growth in maximum throughput for more than five concentrator outputs. Therefore, the impact of input buffer on the maximum throughput of the switch is quite small when we take into consideration that the IOBKS needs five concentrator outputs for meeting the loss requirement 10^{-6} for 99 percent input load.

Table 4. The Maximum Throughput of the IOBKS

L	Maximum Throughput
1	0.632121
2	0.896362
3	0.976663
4	0.995651
5	0.995651
6	0.999905
7	0.999988
8	0.999999

3.3 Delay

The delay at the shared buffer of the KS and the IOBKS can be regarded as the same for the equal load of the switch. the IOBKS another source of delay. As is well known, input buffer allows the head-of-line blocking and thus provides a source of delay. We examine the increased fraction of delay caused by input buffer of the IOBKS.

Let D_s denote the delay experienced by a cell from the time it arrives at an input buffer until it is successfully delivered to the shared buffer. Then, D_s is given by

$$D_s = D_q + T_s \tag{12}$$

where D_q and T_s represent the waiting time and the service time at input buffer, respectively. We will call D_s and D_q the system delay and the queueing delay of input buffer, respectively. Since the time that it takes for a cell to be delivered from input port to shared buffer is one time slot in the KS, the increased delay caused by input buffer in the IOBKS is, therefore, expressed as the following in the unit of time slot.

$$D^+ = D_s - 1 \tag{13}$$

The average queue length of input buffer for finite buffer size s is given by

$$\begin{aligned} \bar{L}_q &= \sum_{i=0}^{s} i\ \Pi_i \\ &= \left(\frac{\rho(1-\beta^s)}{(1-\rho)^2} - \frac{s\rho^s(\alpha+\rho-\alpha\rho)}{1-\rho} \right) \Pi_0 \end{aligned} \tag{14}$$

where Π_i is given in equation (6). Since the service time of cell at input buffer is geometrically distributed with parameter $(1-\bar{\beta})$, T_s, the mean service time, is $1/(1-\bar{\beta})$ and D_q, the mean queueing delay, is $\bar{L}_q/\alpha$. The mean system delay is, therefore, expressed by

$$\bar{D}_s = \bar{D}_q + \bar{T}_s = \bar{L}_q/\alpha + 1/(1-\beta) \tag{15}$$

$\bar{D}^+$, the mean increased delay, can be calculated from the equations (13), (14) and (15). Table 5 shows the mean queue length and the mean increased delay for various input load and the corresponding number of concentrator outputs meeting the loss requirement 10^{-6} and 10^{-10}, respectively, when s=5. As shown in Table 5, $\bar{D}^+$ is less than 0.1 time slot, which is corresponding to only 0.27 μs when line speed of the switch is 155 Mbps. Hence, we can conclude that the increased fraction of delay by input buffer is small enough to have little impact on the delay performance of the switch.

Table 5. Mean Queue Length and Mean Increased Delay by Input Buffer

α	$R = 10^{-6}$			$R = 10^{-10}$		
	L	$\bar{L}_q$	$\bar{D}^+$	L	$\bar{L}_q$	$\bar{D}^+$
0.6	3	0.0098	0.0228	3	0.0098	0.0228
0.7	3	0.0235	0.0433	4	0.0030	0.0055
0.8	3	0.0595	0.0885	4	0.0082	0.0123
0.9	4	0.0285	0.0348	5	0.0039	0.0048
0.99	5	0.0701	0.0715	6	0.0090	0.0092

α : Input Load on the Switch
R : Loss Requirement
L : No. of Concentrator Outputs

4. Concluding Remarks

We proposed an architecture of improving the complexity of the KS, which is called the IOBKS. It was found that the IOBKS could reduce more than 40 percent of switch elements and more than 30 percent of buffers as compared with the KS under the same requirement of cell loss probability of the switch. Moreover, there was no serious problem in other traffic performance measures such as maximum throughput and delay within the switch. Specifically, the IOBKS could achieve a maximum throughput of more than 99 percent with reduced switch elements and buffers, and the increased fraction of delay due to input buffer was sufficiently small enough to be negligible. Therefore, it is expected that the IOBKS can not only save costs but improve the reliability of the switch.

To simplify the analysis, we assumed that traffic is equally distributed through the input and output ports of the switch and that a cell arrievs at input ports in a time-slotted fashion. For the imbablanced traffic and bursty arrivals, traffic performance measures will be degraded more or less in both the KS and the IOBKS. As far as the relative complexity, however, the IOBKS is expected to be superior to the KS in those cases. The details are left for future study.

In the switch with input buffer, it should be judged in advance whether a cell to be transferred is selected or rejected within the switch. In the IOBKS, we would use a method to send the head of a cell to concentrator in advance and to confirm the possibility. For this process, it is required to increase the internal line speed of the switch. This increased overhead should be analyzed and compared with reduced complexity by using input buffer, which is also left for future study.

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