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Silicon-Wafer Direct Bonding for Single-Crystal Silicon-on-Insulator Transducers and Circuits

Gwiy Sang Chung* and Tetsuro Nakamura**

단결정 SOI트랜스듀서 및 회로를 위한 Si직접접합

정귀상, Tetsuro Nakamura

Abstract

This paper has been described a process technology for the fabrication of Si-on-insulator(SOI) transducers and circuits. The technology utilizes Si-wafer direct bonding(SDB) and mechanical-chemical(M-C) local polishing to create a SOI structure with a high-quality, uniformly thin layer of single-crystal Si. The electrical and piezoresistive properties of the resultant thin SOI films have been investigated by SOI MOSFET's and cantilever beams, and confirmed comparable to those of bulk Si. Two kinds of pressure transducers using a SOI structure have been proposed. The shifts in sensitivity and offset voltage of the implemented pressure transducers using interfacial SiO_2 films as the dielectrical isolation layer of piezoresistors were less than -0.2% and $+0.15\%$, respectively, in the temperature range from $-20℃$ to $+350℃$. In the case of pressure transducers using interfacial SiO_2 films as an etch-stop layer during the fabrication of thin Si membranes, the pressure sensitivity variation can be controlled to within a standard deviation of $\pm 2.3\%$ from wafer to wafer. From these results, the developed SDB process and the resultant SOI films will offer significant advantages in the fabrication of integrated microtransducers and circuits.

요 약

본 논문은 SOI트랜스듀서 및 회로를 위해, Si직접접합과 M-C국부연마법에 의한 박막SOI구조의 형성 공정을 기술한다. 또한, 이러한 박막SOI의 전기적 및 압저항효과 특성들을 SOI MOSFET와 cantilever빔으로 각각 조사했으며, bulk Si에 상당한다는 것이 확인되었다. 한편, SOI구조를 이용한 두 종류의 압력트랜스듀서를 제작 및 평가했다. SOI구조의 절연층을 압저항의 유전체분리층으로 이용한 압력트랜스듀서의 경우, $-20℃$에서 $350℃$의 온도범위에 있어서 감도 및 offset전압의 변화는 각각 -0.2% 및 $+0.15\%$이하였다. 한편, 절연층을 etch-stop막으로 이용한 압력트랜스듀서에 있어서의 감도변화를 $\pm 2.3\%$의 표준편차 이내로 제어할 수 있다. 이러한 결과들로부터 개발된 SDB공정으로 제작된 SOI구조는 집적화마이크로트랜스듀서 및 회로개발에 많은 장점을 제공할 것이다.

Ⅰ. Introduction

During the past decade, wafer-bonding techniques have become to the focus of a great deal of research because they provide a powerful and versatile alternative process for improving performance of microtransducers and microactuators fabricated by micromachining. Among various

* 正會員：韓國電子通信硏究所 新素子構造硏究室
(New Structure Devices Section, Electronics and Telecommunications Research Institute)
** 豊橋技術科學大學 電氣・電子工學科
(Dept. of Electrical and Electronic Eng., Toyohashi Univ. of Technology, Japan)
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wafer-bonding techniques,[1~2] anodic bonding has widely used for making pressure transducers and other transducers, in which Si wafers can be bonded to glass substrates by applying electric fields together with an annealing step. However, this technology has following limitations. First, the use of sodium containing glasses precludes the use of the technique from semiconductor device fabrication due to certainly contaminating the Si, so in Si processing environments it can only be tolerated as a finishing treatment. Second, it is subject to built-in stress due to the difference in thermal expansion coefficients between the Si and the glass, and a bonding process at high temperatures of above 400℃. Finally, since the glass can not be etched deeply with high aspect ratio in contrast to Si, it can not give very sophisticated microstructures. Another approach is bonding by fusion or pressing two glass layers of sufficiently low softening point and adapted thermal expansion.[3~4] However, it has a problem of breakdown during the bonding process and in regard to defects increase and impurity profiles distortion.

Two pieces of Si-wafers without any additional glue and with or without surface layers of thermally grown SiO_2 can be bonded together at room temperature without any additional force applied. The term SDB(Si-wafer direct bonding) has been used to avoid confusion with other Si-to-Si bonding technologies. This simple fact occurred at NEC in the early 1960s,[5~6] where it was used to bond discrete transistor chips together. The indispensable conditions to bond two pieces of Si-wafers together are that the surfaces to be bonded have to be clean, flat and hydrophilic, but the wafer fabrication technology at that time was not satisfied with a precondition. Moreover, it was not interesting for application of a SOI (Si-on-insulator) structure to devices. After that, it was ignored over several decades. As one of SOI formation technologies, the formation method of the SOI structure by SDB technology was rediscovered in recent years. In the 1970s, IBM workers began looking seriously at the phenomenon,[7] and in the 1985s they presented as one of the technology for the SOI structure.[8] Almost simultaneously, Toshiba[9] and NavaSensor[10] began publishing information on SDB technology for power devices and Si micromachining, respectively.

Compared with the formation technologies of various SOI structures,[11~13] the SDB technology offers many advantages as follows. First and most important, the crystalline quality of the SOI films,prepared that is comparable to bulk Si and superior to that of other SOI technologies. Second, it provides the capability of realizing sophisticated microstructures completely because fine structure can be made both substrate by micromachining technologies. Third, particularly at elevated temperatures and stress, it have no mechanical and electrical instability due to mismatches in thermal expansion between the dissimilar materials, as well as fatigue in the bonding or gluing agents. Fourth, it does not require the complex fixturing and mechanical limitations of field-assisted bonding processes. Fifth, it admits severe thermal and chemical treatments for bonded Si. Sixth, it can be scaled vertically over a broad range using diffused or epitaxial etch-stop and avoid many of the stress-controlled problems associated with deposited films. Finally, wafer topography permitted, devices contacts and interconnects can be routed on top of the SOI films, avoiding lead transfers and simplifying packaging. Owing to these merits, the SDB technology has been wholeheartedly adopted for fabricating of various useful sensors, actuators and microstuctures, and recognized the importance of the technology at recent years.[14~16]

This paper describes the formation process of a SOI ($Si/SiO_2/Si$) structure by a new developed SDB technology and the electrical and pie-

zoresistive properties of thin SOI films. We also present the characteristics of two kinds of piezoresistive pressure transducers using the insulator of a SOI structure as the dielectrical isolation layer of piezoresistors and an etch-stop layer.

II. Formation process of a SOI structure

In spite of many advantages mentioned above, it is very difficult to obtain a thin, large and uniform SOI layer perfectly. To date, most wafer thinning processes have been performed with mechanical and/ or chemical etching methods. Using only a chemical method, Fujii *et al.*[17] and Petersen *et al.*[18] reported dielectrically isolated pressure transducers fabricated on a SOI structure. In this method, however, signal-processing circuitry fabrication for integrated transducers is impossible to be implemented because of heavy doping concentration. In order to realize intelligent transducers, taking advantages of SOI devices, it is dispensible to the formation of a SOI structure with mirrorlike surface, good flatness and uniformity. The following describes the formation process of a SOI($Si/SiO_2/Si$) structure by SDB technology as shown in Fig. 1.

1. Bonding procedure

Among variously important considerations in the preparation of a SOI structure by SDB technology, first of all bonding has to be homogeneous over the entire interface without the presence of unbonded areas or bubbles, also referred to as voids. The existence of voids must be weak the average bonding strength at the interface and limit the yield of devices fabricated in such materials. The voids appearing in the bonding process can be caused by insufficient wafer flatness, surface damage and trapped gases between wafers or dust particles remaining on the wafers. The voids generated in this step remain nearly unaffected during high-temperature treatment. However, the voids appearing in the annealing step, which have first been observed by Shimbo *et al.*[9], and late Ohashi *et al.*[14], form during annealing at 200℃, grow in size and number up to about 800℃ and disappear above about 1000℃. Therefore, the voids causing the annealing step may be avoid by thermal annealing at high temperatures of above 1000℃. In this time, we had tried the wafer bonding by two methods. One is bonding under normal conditions, e. g., at room temperature and atmospheric pressure, and subsequently thermal annealing at elevated temperatures, and the other is bonding *in situ* in the same oxidation furnace after oxidation, and subsequently annealing treatment at high temperatures.

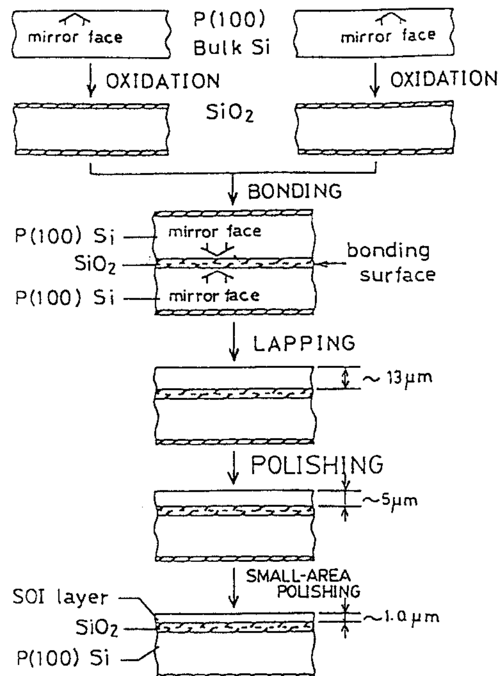

Fig. 1. Fabrication process of a SOI structure.

The Si wafers used in this work were 2 or 4-inch diameter (100) Czochralski-grown polished single-crystal Si wafers, whose flatness and roughness were similar to those utilized in integrated circuits, with various boron or phosphorous doping. These wafers were available commercially and flat enough to avoid voids formation due to insufficient surface flatness.

The bonding process under the normal conditions is as following. After standard initial cleaning, thermal oxide with 1100Å thickness was grown on the wafers in steam at 1000℃ in standard furnace. Then, in order to activate OH-groups on the SiO_2 surfaces, the wafers dipped in a diluted HF solution, rinsed in DI water and spin dried by a centrifuge. Immediately after hydrophilic treatment, two wafers to be bonded were placed in a vacuum chamber for several minutes. Afterwards the two wafers was brought into contact face-to-face with the mirror-polished surfaces in the vacuum chamber at room temperature and without any external pressure. During this process, the final position of the wafers is fixed by attractive interaction between the hydrophilic surfaces. The bonded wafer was heat treated at 1000℃, without applying a weight and for 30 minutes in wet ambients. in order to avoid causing due to particle contamination, all bonding procedures were performed in a clean room environment.

On the other hand, the bonding process by the second method is as followings. Starting materials were identical to Si wafers used in the normal bonding. After growing thermal oxide with 1100Å thickness, the bonding process was performed *in situ* in the same oxidation furnace at 1000℃ and the bonded wafer heated 30 minutes in wet ambient.

2. Thinning

Following bonding process, the voids at the bonding interface were observed by ultrasonic flaw detection and transmission x-ray topography. High-resolution TEM was also used to investigate the bonded interface prepared by these processes. Then, in order to obtain thin SOI films, one side of the void-free bonded Si wafer was thinning, which consists of three steps as followings : the lapping, the M-C(mechanical-chemical) polishing and the M-C local polishing.

At first, the one side of the completely bonded Si wafer was roughly thinned by conventional lapping process using powder #1000 and #2000. The thickness of the SOI layer was controlled by measuring the thickness of the bonded wafer sometimes. Until the thickness of the remaining SOI layer was within 15μm, the lapping process was repeated. Next, the residual Si surface was chemically etched with HF-HNO_3 to remove any disturbed surface introduced by the lapping process, in which the thickness of the SOI layer was 13 μm.

After that, the SOI layer was further thinned by the conventional M-C polishing process using the slurry composed of colloidal silica : 5% KOH solution=1 : 1. The resultant thickness of the thinned SOI layer by means of the conventional M-C polishing were approximately 5 μm with standard deviation of 1μm.

Finally, a uniform, mirrorlike and large area SOI layer was obtained by a newly developed CCP(computer controlled polishing) system. The block diagram of the CCP system is shown in Fig. 2. The system consists of a polishing machine with a small-area tool, a film-thickness profiler and a microcomputer. Our process involves segmentation of a wafer surface into small cells, measurement of film-thicknss, and local polishing in each cell. The pressure applied to the tool, as well as the lateral motion of the tool, were controlled by the microcomputer. After one cycle of polishing process was run, the thickness distribution was measured by the film-thickness which calculates the thickness of thin films from period-

ic dependence of reflectance on wave lengths ranging from 4000Å to 8000Å. And the new data was fed back to the computer in order to correct the distribution of polishing pressure. This error-correction loop repeated until the SOI layer of a uniform 1μm-thick was achieved. The polishing tool, which was spining, was moved over the wafer by moving the sample stage in x and y directions. The diameter of the tool head was 16 mm and a polyurethane square pad was attached to its surface. Until SOI thickness became to 5 μm, ZrO_2 powder was used as an abrasive for rough polishing and the identical powder used the M-C polishing was used during the final M-C local polishing. The M-C local polishing was repeated until a uniform SOI layer was achieved. Thus, we obtained the SOI layer with a mirrorlike surface, which is uniform in thickness to 30% or better (e.g., ±0.15 μm on a 1.0μm final layer) on a 4-inch wafer area. This uniformity is adequate for most sensing and MOS device applications, and it could be improved with tighter process control.

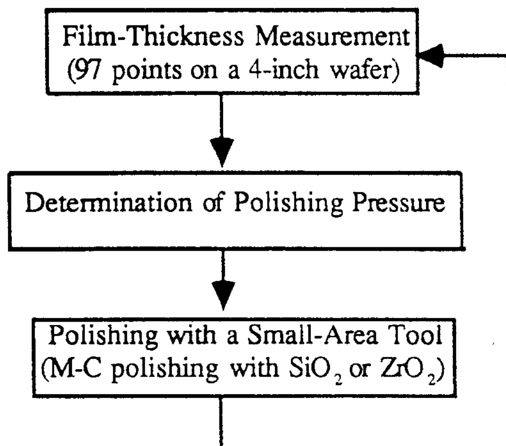

Fig. 2. Block diagram of CCP system.

Ⅲ. Evaluation of thin SOI films

1. Bonding interface

In the fabrication of a SOI structure by SDB technology, it is very important to reduce the voids at the bonding interface between two wafers, since parts of the voids are peeled up during the lapping and polishing process due to thinning of the SOI layer. The typical ultrasonic flaw images of the bonded wafer are shown in Fig. 3. Fig. 3(a) shows the ultrasonic flaw image of the bonded wafer that was performed at room temperature and atmospheric pressure, and subsequently annealing treatment at elevated temperatures, in which voids were observed. Here, the voids was shown by the white areas because the ultrasonic wave was reflected at the void. Fig. 3(b) shows the ultrasonic flaw image of the bonded wafer that was performed *in situ* bonding after thermal oxidation, and immediately thermal annealing at high temperatures in all same furnace, which shows perfect bonding over all of the wafer surface. Using the latter method, we achieved Si-wafer bonding without voids.

Among various causes generating voids, the voids appearing by trapped gases or particles remaining on the wafers may be avoided by bonding *in situ* oxidation furnace performed rather than the normal bonding in this work. The most probable contamination is thought to be hydrocarbons on polished Si wafers in conjunction with wafer manufactures. Therefore, the voids appearing during annealing step should be avoidable by getting rid of adsorbed hydrocarbons before wafer bonding. Wet cleaning is one method to remove hydrocarbons, but it can not eliminate them completely. Since above 800℃ all hydrocarbons contamination Si surfaces have been desorbed,[19] pre-bonding annealing is another possibility to reduce the hydrocarbon content at Si surfaces. Compared with any other bonding processes recently reported,[20~21] the bonding me-

thod proposed in this work can be avoidable the voids generating during the bonding process completely.

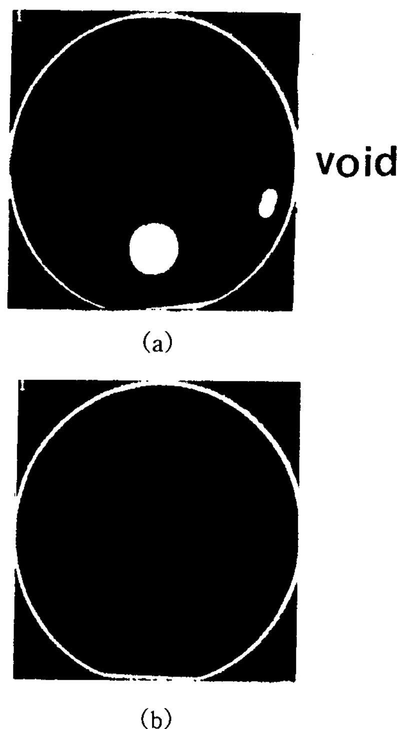

Fig. 3. Ultrasonic flaw images of bonded wafer (a) at room temperature and atmospheric pressure and (b) in oxidation furnace.

The bonding mechanism of the two SiO_2 films was originally explained Lasky.[8] He proposed that after bonding of the two SiO_2 sufraces with silanol groups(=Si-OH) formed on each of the SiO_2 surfaces by activation treatment, the two SiO_2 surfaces can be bonded by polymerization of silanol groups(=Si-O-Si=) in the process of annealing at elevated temperatures. We also consider the *in situ* bonding process in the oxidation furnace to be the same as the Lasky bonding process.

2. Bonding strength

The bonding of two SiO_2 surfaces depends on heating treatment temperature.[9] We measured the bonding strength of a bonded wafer by a tensile tester, in which samples cut as dimensional size of 1 cm were used. Fig. 4 shows normalized bonding strength as a function of heating treatment temperature. In spite of contacting only at room temperature and under atmospheric pressure, the bonding strength of the bonded wafer is sufficiently large(2-5kg/cm²) for wafer handling because of Van der Waals force between wafer surfaces. At above 200℃, the bonding strength increased with increasing heating treatment temperature, but in the temperature range of between 400℃ and 800℃ the bonding strength was saturated once. However, after thermal treatment at high temperatures of 1000℃ the bonding strength increases with an increasing of annealing temperature, finally reaching the fracture strength of single-crystal Si body (100-200kg/cm²) after thermal treatments at high temperatures of above 1000℃ the bonding strength corresponds to the fracture strength of single-crystal Si body.

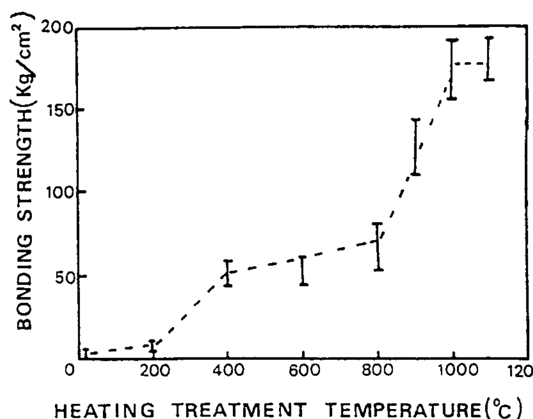

Fig. 4. Bonding strength as a function of heating treatment temperature.

From these results, the bonding process presented here requires the high temperature heat treatment of above 1000℃. For application the advantages of SDB technology to sophisticated microdevices, it must research bonding method at low temperature because of the offer of much flexibility in fabrication processes.

3. Built-in stress

Built-in stress caused by the lapping and polishing process during the formation of a SOI structure was measured using microscopic Raman spectroscopy.[22] The Raman spectra measurements were made at room temperature using a back-scattering configuration source. The error of Raman shift was 0.05 cm^{-1} and the spatial resolution was 0.8 μm diameter. Fig. 5 shows the typical Raman spectra of the 1.0 μm-thick SOI films and the bulk Si. The difference between the peaks is 0.51 cm^{-1} and exhibits a shift to a lower frequency. This corresponds to the tensile stress for the SOI films, which is estimated to be about 1.26×10^9dyn/cm^2.

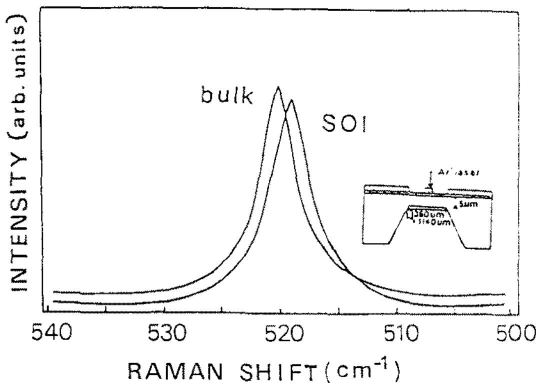

Fig. 5. Typical Raman spectra of bulk Si and a 1.0μm-thick SOI layer.

Moreover, we measured the dependence of built-in stress on the thickness of the SOI layer. The stress distribution as a function of SOI thickness prepared by SDB technology is shown in Fig. 6. The built-in stress decreases as the thickness of the SOI layer increases, and consequently over 10.0μm, the sterss residing on the SOI layer become almost stress free. On the other hand, using the SOI structure with 5μm-thick SOI layer, we investigated whether the built-in stress actually affected the membrane deflection on before or after the membrane formation., The result shows almost no difference because the membrane dimensions (360μm×1140μm) with the clamped edge are very small.

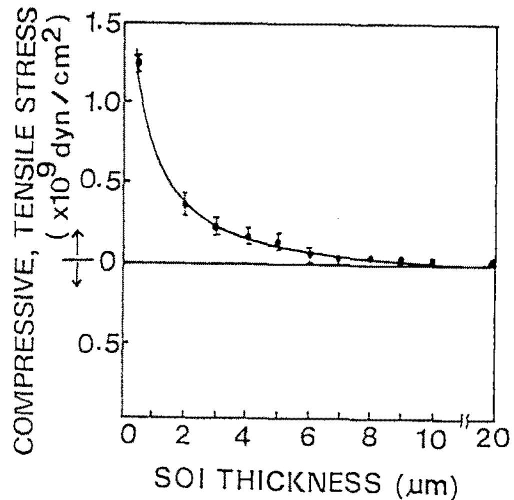

Fig. 6. Stress distribution as a function of the thickness of a SOI layer.

4. SOI MOSFET's

For device applications integrated into a sensing-element and signal-processing circuitry on one chip, SOI MOSFET's were fabricated on the SOI films by a standard poly-Si gate process except for a Si island process. With the SiO_2 layer used as an etch-stop layer, the dielectrical isolation of the SOI layer was performed by wet etching in a KOH solution at 40℃. Fig. 7(a) and (b) indicated MOSFET characteristics of drain current-drain voltage (I_D-V_D) at a drain voltage of 75mV, respectively, where the gate length/width ratio(L/W) is 40/50 μm. In the case of thick (8000Å) SOI films, the MOSFET characteristics are nearly the same as those of a bulk Si except for a kink effect of I_D-V_D : threshold voltage(0.48V), effective mobility (763cm^2/V.S) and subthreshold swing (113mV/dec). However, the MOSFET characteristics fabricated on the thin (2500Å) SOI films showed better characteristics than those of bulk Si and thick SOI films : threshold voltage (0.1V), effective mobility(857cm^2/V.S) and subthreshold swing (89

mV/dec). From these results, it is possible to eliminate the kink effect and the mobility enhancement by thinning of the SOI layer,[23] and to implement the signal-processing circuitry for high-temperature integrated transducers. It is evident that the thin-film SOI MOSFET's offer certain noteworthly advantages over bulk MOSFET's. Moreover, these electrical characteristics are superior to those obtained from other SOI technologies. It is very important to improve the thinning and uniformity of SOI layer to obtain good electrical characteristics in MOFET's.

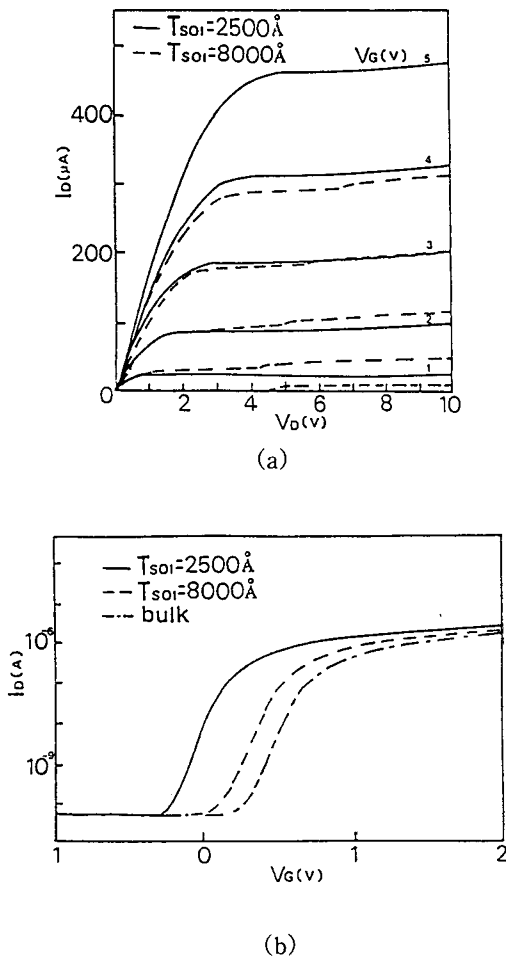

Fig. 7. Transistor characteristics of MOSFET :
(a) drain current-drain voltage(I_D-V_D) ;
(b) drain current-gate voltage(I_D-V_G) of MOSFET.

5. Piezoresistive properties

Among various advantages of a SOI structure, using the insulating layer of the SOI structure as the dielectrical isolation layer of devices will offer most important merit. Especially, the dielectrical isolation of piezoresistors in piezoresistive pressure transducers can be used at higher temperature environments than piezoresistors with pn junctions.

The temperature dependence of a dielectrically isolated resistor with dimension of 60μm×60 μm on the SOI structure was measured in the temperature range of from −20℃ to +350℃. Fig. 8 shows the TCR (temperature coefficent of the resistance) of dielectrically isolated resistor on the SOI structure as a function of boron doping concentration. The TCR varied from 1000 ppm/℃ to 2400 ppm/℃, corresponding to the doping concentration in the measured temperature range, which is similar to that of bulk Si. These values are much lower than the TCR of the resistor reported by Bullis *et al.*.[24] This result testifies that a piezoresistor using the SiO_2 layer of a SOI structure as a dielectrical isolation layer can be used at higher temperatures.

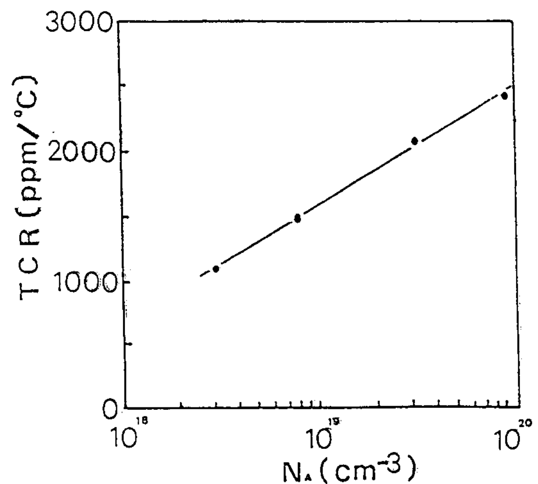

Fig. 8. Temperature characteristics of a dielectrically isolated resistor as a function of boron doping concentration in the temperature range of −20℃ to +350℃.

The piezoresistive effect, i. e., the relative change of resistance with the applied strain, in the thin films can be described by a gauge factor (K). For determination of the gauge factors, cantilever beams (30mm×5mm×0.25mm) diced from the SOI wafer were used.[25] The strain is generated on the resistor of the Si islands (200μm×60μm) by bending on the SOI beams. Fig. 9 shows the percentage change in resistance as functions of strain and boron doping concentration for longitudinal (i. e., direction of strain is parallel to current), transverse(i. e., strain is perpendicular to current) and shear (i. e., strain is applied with angle 45° to current) piezoresistor. The resistance changed linearly against the strain. The estimated gauge factors (longitudinal gauge factor K_l, transverse gauge factor K_t and shear gauge factor K_S) at 25℃ were comparable to those of bulk Si for the carrier concentration of from $3\times10^{18}cm^{-3}$ to $1\times10^{20}cm^{-3}$. From the above results, the built-in stress residing on the SOI film formed by SDB technology can be ignored. When the design and process of sensing-elements have been considered using the SOI wafer prepared

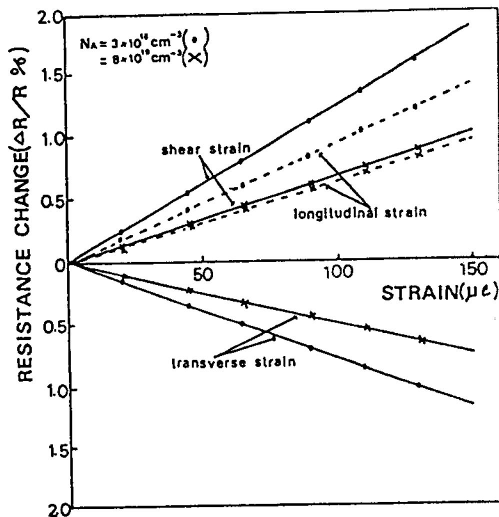

Fig. 9. Graph of percentage change in resistance as functions of strain and boron doping concentration for piezoresistors fabricated on thin SOI films.

by the method presented by in this work, it will possible to handle the SOI wafers in the same manner as bulk Si wafers.

The temperature dependence of the gauge factor was measured in the temperature range of from −20℃ to +100℃. Fig. 10 shows the boron doping dependence of the temperature coefficient of the gauge factor (TCK_l, TCK_t and TCK_S). Compared with bulk Si, the temperature dependence of the gauge factor has been observed to exhibit similar behavior to that of bulk Si. However, the TCK_t is changed only slightly more than the TCK_l and TCK_s over the range of doping concentration, with a small decrease in the examined range.

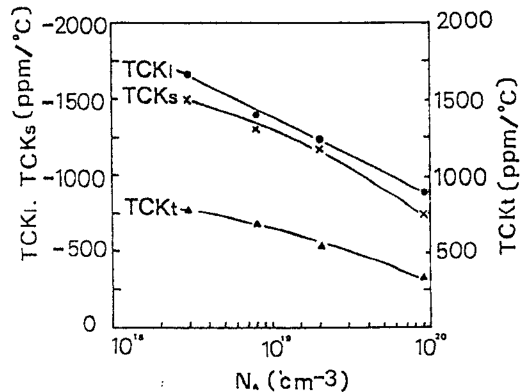

Fig. 10. Temperature coefficients of gauge factor (TCK_l, TCK_t and TCK_S) as a function of boron doping concentration in the temperature range of from −20℃ to +100℃.

Ⅳ. Application to pressure transducers

Pressure transducers were fabricated on a $Si/SiO_2/Si$ structure prepared by the method described above. In the conventional piezoresistive pressure transducers, the longitudinal and transverse piezoresistive effects in the form of a Wheatstone bridge are utilized. However, from the values of the gauge factor shown in Fig. 9, it is clear that the sensitivity of a pressure transducer utilizing only the shear piezoresistive effect

is almost the same as that of a conventional one. Furthermore, it would offer the advantages of stability, low offset voltage drift, low linearity deviation, miniaturization of devices and ease of production because of the utilization of only one piezoresistor. Therefore, we used a single-element four-terminal piezoresistor, which is placed at the center of a rectangular membrane because of the highest stress distribution.[26] On the other hand, all piezoresistors are inclined at an angle of 45° to the ⟨100⟩ direction in a p-type Si(100) crystal surface.[27]

When the stress is applied on the piezoresistor, a transverse electrical field can be developed by a longitudinal current. Accordingly, the maximum output voltage V_{out} taken out from electrodes 3 and 4 of the piezoresistor as shown in Fig. 11 is derived under the conditions mentioned above.

$$V_{out} = (W/L)V_S(1-\nu_{si})(\pi_{44}/2)f(Pb^4/a^4+b^4)(a/h)^2[1-(a/b)^2]$$

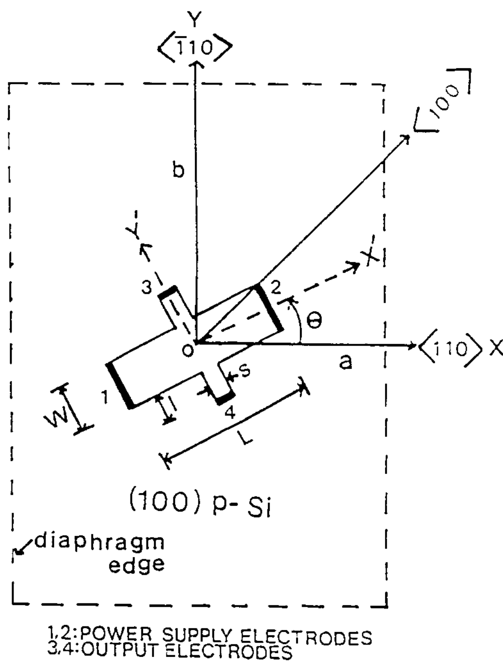

Fig. 11. Schematic design of a single-element four-terminal piezoresistor.

where W, L are the length and the width of the piezoresistor, V_S is the supplied voltage, π_{44} is the component of the piezoresistive coefficient corresponding to shear stress, f is the correction factor caused by the short-circuit effect of the electrodes, P is the pressure exerted on the membrane, L is the thickness of the membrane, and a, b are the lengths of the membrane on the x, y axes, respectively.

The doping concentration of the piezoresistor was $N_A = 3\times10^{18}cm^{-3}$; the measured shear gauge factor at this doping concentration was about 121. The membrane and the dielectrical isolation of the piezoresistors were formed by wet etching in a KOH solution. The dimension of the membrane and its thickness were 360μm×1140μm and 5μm respectively.

Piezoresistive pressure transducers have several factors influencing device performance degradation.[28] To eliminate not only thermal stress, but also occasional influence of mechanical tensions caused by encapsulation in these factors, all measurements were performed on the devices, i. e., before the wafer was diced into individual devices, and mounting was also performed at room temperature using a polyimide.

1. High-temperature pressure transducer

The operating temperature range of the conventional diffused or implemented piezoresistive pressure transducers is limited to a relatively low temperature due to the leakage current of the pn junction at elevated temperatures.[29] To overcome this drawback, pressure transducers using a SOI structure are effective, since they are able to operate in a higher temperature region because the piezoresistors are dielectrically isolated by the insulator of the SOI structure.

Using a SiO_2 layer as the dielectrical isolation of piezoresistors in a SOI structure perpared through the method described above, we developed SOI pressure transducers. Fig. 12 shows the

temperature characteristics of the pressure sensitivity and the offset voltage in the implemented transducers. The shifts in sensitivity and offset voltage are less than −0.2% and +0.15% in the temperature range of from −20°C to +350°C.

The result of this shift in the pressure sensitivity corresponds to less than 13mV thermal offset voltage shift. The piezoresistive pressure transducer has several temperature drift mechanisms which contribute to the high-temperature coefficients. The temperature variation of the pressure sensitivity depends on the temperature dependence of the piezoresisitive coefficients, which are inversely proportional to the temperature if there are no parasitic effects such as stress or temperature leakage current. The measured piezoresistive coefficient π_{11} has been found to be 82×10^{-11}m²/N at room temperature, which is in good agreement with the theoretical value of bulk Si.[31] The temperature coefficients of the sensitivity in the implemented transducers are comparable with the dependence of the temperature coefficient of the piezoresistive coefficient($TC\pi$), which agrees very well with the temperature up to 350°C. From these results, it is evident that the effect of built-in stress caused by the M-C polishing can be ignored. Therefore, the temperature drifts of the fabricated transducers are dominately by the temperature dependence of the piezoresistive coefficient π_{11} due to the dielectrical isolation of a piezoresistor.

Since the dimensions of a piezoresistor are four times smaller than a conventional one, the implemented transducers can less the effects of thermal stress and stress averaging due to the fluctuation of surface doping concentration. Therefore, the temperature dependence of the offset is relatively small. On the other hand, stability is a very important factor in high-temperature capability. The resistance instability is less than 0.04% error during thermal cycles over hundreds of hours at 350°C. Therefore, the dielectrically isolated single-element four-terminal piezoresistor is very useful as a high-performance sensing-element for high-temperature operation.

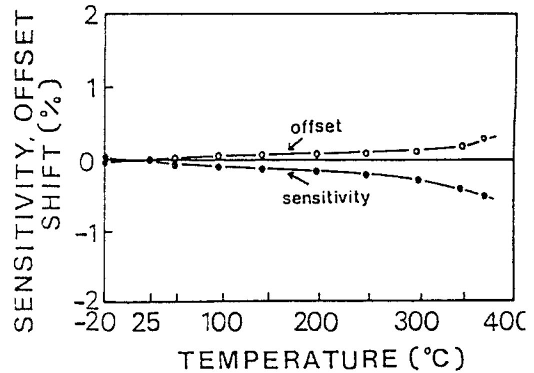

Fig. 12. Temperature characteristics of pressure transducers using the insulator layer of a SOI structure as the dielectrical isolation layer of piezoresistors.

The characteristics of fabricated transducers using the SiO_2 layer of a SOI structure as the dielectrical isolation layer of piezoresistors are summarized in Table 1.

Table 1. Typical output characteristics of SOI pressure transducers using the insulator of a SOI structure as the dielectrical isolation layer of piezoresistor

Pressure range	0~700mmHg
Supply voltage	5VD.C
Sensitivity	0.039mV/V.mmHg
Nonlinearity	+0.18%FS
Hysteresis	+0.05%FS
Temperature range	−20~+350°C
Dependence of sensitivity	−0.2%
Dependence of offset voltage	+0.15%

2. High-resolution pressure transducer

Approches to tactile imaging devices to enable them to measure not only force but also force distribution have been based on Si membrane pressure transducers using the array of either piezoresistive or capacitive cells. For the piezoresistive pressure transducer, control of the pressure sensitivity has been difficult because it is

inversely proportional to the square of the membrane thickness. Therefore, accurate control of the membrance thickness is very important to enable the realization of high-resolution pressure transducers with invariant pressure sensitivity on a large area.[31]

In this section, the advantages of useful micromachined Si structural control are demonstrated by applying the SiO_2 layer of a SOI structure to an etch-stop layer during the fabrication of thin Si membranes, in which the membrane thickness can be accurately determined by the thickness of SOI layer. Fig. 13 shows a histogram of the pressure sensitivity variation measured at constant voltage of 5V. The histogram included 200 devices, relative to the average value. The average pressure sensitivity was 133 mV and the standard deviation was only 2.3%. This is a great improvement as compared to previous fabrication methods of pressure transduers.[32] The piezoresistive pressure transducers have many factors that affect the pressure sensitivity variation : the membrane thickness, the membrane size, the alignment error of the piezoresistive coefficient π_{44} variation due to the impurity concentration variation fabricated devices.[28] Howere, in the case of the fabricated pressure transducers, the pressure sensitivity variation caused by the fluctuation of the membrane thickness can be ignored because of the control of the membrane thickness by the SOI layer.

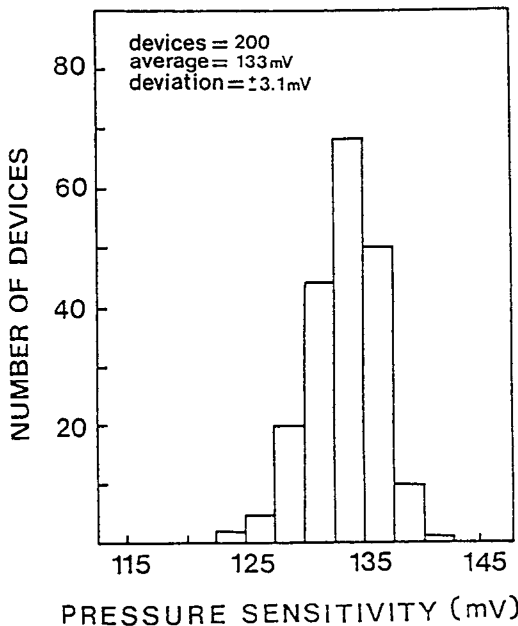

Fig. 13. Histogram of pressure sensitivity variation in the implemented pressure transducers using the insulator layer of a SOI structure as an etch-stop layer.

The characteristics of fabricated transducers using the SiO_2 layer of a SOI structure as an etch-stop layer during the fabrication of thin Si membranes are summarized in Table 2.

Table 2. Typical output characteristics of SOI pressure transducers using the insulator layer of a SOI structure as an etch-stop layer

Pressure range	0~700mmHg
Supply voltage	5VD.C
Sensitivity	0.04V/V.mmHg
Nonlinearity	+0.16%FS
Hysteresis	+0.05%FS
Pressure sensitivity variation	±2.3%s.d
Temperature range	−20~+120℃
Dependence of sensitivity	−0.3%
Dependence of offset voltage	+0.2%

V. Conclusions

The developed SDB is very useful process technology for a uniform, thin and large single-crystal SOI structure formation. It was confirmed that the electrical and piezoresistive properties of the resultant thin SOI films were comparable to those of bulk Si. Therefore, it will be possible to handle the SOI wafers prepared by the process described in this paper in the same manner as bulk Si.

In case of pressure transducers using SiO_2 films as the dielectrical isolation layer of piezoresistors in the SOI structure, the implemented pressure transducers can be operated at high temperatures up to 300℃. Moreover, as it is possible to integrate a signal-conditional circuitry, ta-

king advantages of thin SOI devices, the developed pressure transduers are very suitable for the development of high-temperature integrated pressure transducers.

On the other hand, the standard deviation of the implemented devices using SiO_2 films as an etch-stop layer during the fabrication of thin Si membranes was only 2.3% over 200 devices. The SOI structure presented here is very promising materials for the development of high-resolution pressure transducers with no-variation pressure sensitivity on a large area. Therefore, these devices seem to be especially attractive for application such as tactile imaging devices.

Instead of surface micromachining using poly-Si or Si_3N_4 films, surface micromachining of a SDB process proposed here will also provide powerful and versatile alternative process for realizing many types of microtransducers, microactuators and microstructures.

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著 者 紹 介

GwiySang Chung was born in Kyongnam, Korea, on June 20, 1961. He recevied B.S. and M.S. degrees in electronic engineering from Yeungnam University, Kyongsan, Korea, in 1983 and 1985, respectively and a Ph.D. degree from Toyohashi University of Technology, Toyohashi, Japan, in 1992. He is currently a research engineer with New Structure Devices Section, Electronics and Telecommunications Research Institute. His research interests include SOI and solid-state mechanical transducers and actuators. Dr Chung is a member of the Korea Institute of Telematics and Electronics Korean Sensors Society, and the Institute of Electronics, Information and Communication Engineers of Japan.

Teturo Nakamura was born in Nigata, Japan, in 1932. He received his B.E. and Ph.D. degrees in electrical engineering from Tohoku University. Sendai, Japan, in 1957 and 1968, respectively. He joined NEC, Kawasaki, Japan, in 1957, where he worked on Ge alloy-type switching transistors, Si high-frequency high-power transistors, microwave diode and diffusion processes on Si. Since 1978 he has been with Toyohashi University of Technology, where he is now a professor. His current research interests are in semiconductor sensors. Dr Nakamura is a member of the Institute of Electrical Engineers of Japan, the Japan Society of Medical Electronics and Biological Engineering, the Institute of Electronics, Information and Communication Engineers of Japan, and the Japan Society of Applied Physics.