Jitter Analysis for the PLL in the Baseband Signal

(베이스 밴드 신호에서 PLL에 대한 지터 해석)

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要 約

입력 단극성 NRZ(Nonreturn to zero) 신호의 트랜지션 게이팅(transition gating)에 의한 PLL회로의 지터(jitter) 발생을 고려하여, 타이밍 복원회로의 시불변 선형 등가 회로를 유도하였고, 중계단에 따라 누적되는 지터(jitter)의 크기를 구하였다. 90Mbps 광통신 수신기에 대한 전자 계산기 모의 실험을 수행하여, 제 1 단에서는 −5.1766dB의 정렬 지터(alignment jitter)와 누적지터(accumulated jitter)가 제 7 단에서는 −1.0193dB의 정렬지터(alignment jitter), 4.9053dB의 누적 지터(accumulated jitter)가 생성됨을 확인하였다.

Abstract

Considering transition gating of the input unipolar NRZ signal, the equivalent linear time-invariant model has been derived for the PLL in the timing clock recovery circuits. The magnitude of the alignment and accumulated jitter has been found along a chain of repeaters.

For the timing recovery circuit of 90 Mbps optical communication system, the computer simulation shows that, for the first stage of the chain, the alignment jitter and the accumulated jitter are of −5.1766 dB and for the 7-th stage, the alignment jitter and accumulated jitter have the value of −1.0193 dB, 4.9053 dB respectively.

I. Introduction

In digital/optical receivers or repeaters, the timing clock recovery is required for the original data to be found from the input data stream. Self-timing method is very useful for the clock recovery, in which there are two schemes: tuned-circuit scheme and PLL scheme. [1][2][3]

CCITT defines the jitter as "a short-time variation of the significant instants of the digital signal position from their ideal pulse position in time." Jitter can be produced in most cases, but the significant parts of the jitter sources are the multiplex/demultiplex, timing clock recovery circuits. The dominant jitter component of the multlplex/demultiplex is the waiting time jitter. [1][2]

In this paper, considering transition-gating, the equivalent linear time invariant model for 2-nd order PLL has been derived, and the

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jitter phenomena in the equivalent model and the mathematical accumulation dimension have been analyzed.

The PLL timing recovery circuit in the previously implemented 90 Mbps optical communication system [6] was adapted to this equilvalent model, and through the computer simulation the magnitude of accumulated jitter could be found provided that the used PLL circuits are all the same in the chain of repeaters.

II. Linear Time-Invariant Model for the PLL

The general PLL model for the timing extractor is shown in Fig. 1. [1] [5].

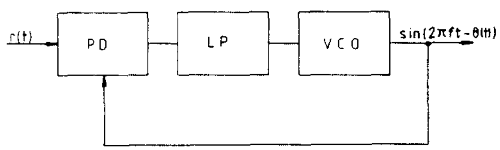

Fig. 1. General model of PLL.

The input signal of the PLL is as follows.

$$r(t) = \sum_k a(k)\, f[t-kT-\phi(k)] + n(t) \qquad (1)$$

where $\{a(k)\}$ is the NRZ data with ±1,

$\phi(k)$ is the phase of input data,
$n(t)$ is noise.

And $\theta(t)$ in Fig. 1 is the output timing-phase. The output error signal of the phase detector such as zero-crossing phase detector, dead-zone quantizer phase detector can be shown eq.(2).[4]

$$e(k) = Kp\, d(k)\, [\theta(k) - \phi(k) - w(k)] \qquad (2)$$

Where d(k) has the value of 1 or 0 according to the data transition, Kp is the transfer gain of PD(phase detector), and w(k) represents phase variation on the influences of ISI(intersymbol interference) and channel noise. After the period T is normalized to 1 as unit interval, by use of eq.(2), the error signal of phase detector is expressed in eq.(3).

$$e(t) = \sum_k e(k)\, \delta(t-k) \qquad (3)$$

Using the eq.(2) for the phase detector, we can obtain the improved model of Fig. 2 from the general model Fig. 1.

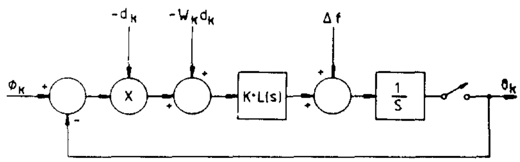

Fig. 2. Improved model of PLL.

Δf is the detuning frequency, VCO(voltage controlled oscillator) acts as the integrator for the input signal, L(s) is the transfer function of the loop filter, L(0)=1. For the PLL,

the open-loop gain K is KpKvL (0),
Kp is the transfer gain of the phase detector,
Kv is the transfer gain of the VCO,
L(0) is the DC gain of the loop filter.

The model of the Fig. 2 is linear, but time-varing because of the transition-gating variable d(k).

$$(\phi(k) - \theta(k))\, d(k) = (\phi(k) - \theta(k))\, p + (\phi(k) - \theta(k))\, (d(k) - p) \qquad (4)$$

$$p = E\{d(k)\} \qquad (5)$$

Where E{ } represents the expectation value, and p is equal to 0.5 in equiprobable case of digital data.

The first term of the right hand side of eq.(4) is the low frequency response to the phase detector, the second term is the wide-band noise generated by gating which produces the jitter for the signal.

If VCO (voltage controlled oscillator) has the static offset of u,

$$E\{(\phi(k) - \theta(k))\} = u \qquad (6)$$

Using the eqs.(5) and (6), the eq.(4) can be replaced by eq. (7).

$$\{\phi(k) - \theta(k)\}\, d(k) = (\phi(k) - \theta(k))P + (d(k)-p)u \qquad (7)$$

In Fig. 2 the detuning freq. Δf can be replaced by $-\Delta f$.

In order for the PLL to be in the lock-state, the input of the loop filter L(s) must be $\Delta f/K$, at this time let's average each signal at the phase detector output stage.

$$\begin{aligned}\overline{(\phi(k) - \theta(k))\, d(k)} &= \Delta f/K + \overline{w(k)\, d(k)} \\ &= \Delta f/K + \overline{w(k)\, d(k)} \\ &= \Delta f/K \qquad (8)\end{aligned}$$

Since $E\{w(k)\}$ is equal to zero, the above eq. (8) can be obtained. The left hand side of eq. (8) will be described as follows by use of eqs. (5), (6).

$$\begin{aligned}\overline{(\phi(k) - \theta(k))\, d(k)} &= \overline{(\phi(k) - \theta(k))}\;\overline{d(k)} \qquad (9) \\ &= up\end{aligned}$$

From the eqs. (8), (9), the static offset u is

$$u = \Delta f/pK \qquad (10)$$

Of course, $(\phi(k)-\theta(k))$ and d(k) are uncorrelated, w(k) d(k) is the function made by noise, data and is mutually independent and stationary.

The linear time-invariant model of the PLL is described in Fig. 3 by taking the z(k) as eqs. (11) and (12).

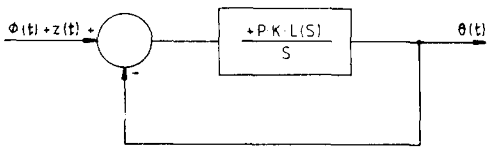

Fig. 3. Linear time-invariant model for PLL.

In Fig. 3, z(t) is represented as follows,

$$z(k) = (-1/p)\{w(k)\, d(k) + u(d(k) - p) + \Delta f/K\} \qquad (11)$$

$$z(t) = \sum_k z(k) \cdot \delta(t-kT-\lambda) \qquad (12)$$

The global transfer function of linear time-invariant model for the PLL can be represented as following eq. (16).

$$H(s) = \frac{p\,K\,L(s)}{s + p\,K\,L(s)} \qquad (13)$$

III. Repeater Chain

After the spectrum and variance of the $\theta(t)$ are determined, the accumulated jitter can be quantitatively calculated for the case of repeater chain.

$$S_\theta(f) = |H(f)|^2\, S\phi(f) + |H(f)|^2\, Sz(f) \qquad (14)$$

where $S_\theta(f)$ and Sz(f) are the spectral density of $\theta(t)$, z(t) respectively.

$$z(t) = \sum_k z(k) \cdot \delta\,(t-kT-\lambda) \qquad (15)$$

z(t) is stationary and λ is random variable distributed with [0, T].

Because H(f) has the characteristic of LPF, Sz(f) can be approximately expressed as Sz(0).

$$S_\theta(f) = |H(f)|^2\, S\phi(f) + |H(f)|^2\, Sz(0) \qquad (16)$$

and the variance of the $\theta(t)$ is

$$\sigma_\theta^2 = \int |H(f)|^2\, S\phi(f)\, df + Sz(0) \int |H(f)|^2\, df \qquad (17)$$

The second term in eq.(17) is the jitter factor which is continuously appeared in PLL timing extractor.

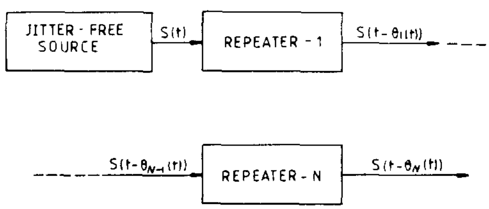

Fig. 4. Theoretical model of repeater chain.

Fig. 4 is the block-diagram that shows the jitter accumulation in repeater chain and at first stage the jitter-free signal is received.

Fig. 5 is the block-diagram which shows the jitter accumulation along a chain of the same repeaters for the equivalent model derived from section II.

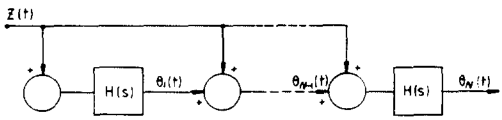

Fig. 5. Analytical model of repeater chain.

The difference jitter magnitude $\Delta_N(t)$ is

$$\Delta_N(t) = \theta_N(t) - \theta_{N-1}(t) \tag{18}$$

which is the jitter produced only in the N-th stage.

In Fig. 5, it is assumed that PLL as the timing extractor has the identical property in each stage. Starting from the first stage receiving jitter-free signal to the N-th stage, the power spectral density and variance of the alignment jitter and accumulated jitter are expressed in the form of eqs. (19), (20), (21), (22).

$$S_{\Delta_N}(f) = \int |H^N(f)|^2 \, Sz(0) \tag{19}$$

$$\sigma^2_{\Delta_N}(f) = \int |H^N(f)|^2 \, Sz(0)\, df \tag{20}$$

$$S_{\theta_N}(f) = \sum_{K=1}^{N} |H^K(f)|^2 \, Sz(0) \tag{21}$$

$$\sigma^2_{\theta_N}(f) = \int \sum_{K=1}^{N} |H^K(f)|^2 \, Sz(0)\, df \tag{22}$$

IV. PLL of 90 Mpbs Optical Communication System

The implemented 90 Mpbs system has the 2-nd order PLL which is used as timing clock recovery circuit and has the 1-st order loop filter.

The loop filter circuit is shown in Fig. 6.

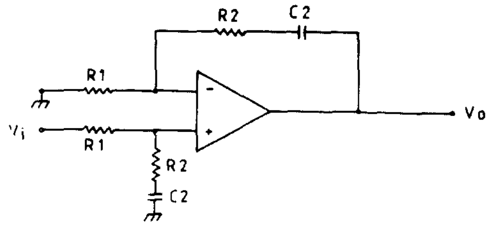

Fig. 6. Loop filter of PLL in optical system.

In order to develop the transient response, we place the RC LPF in front of loop filter. The improved circuit of loop filter is shown in Fig. 7.

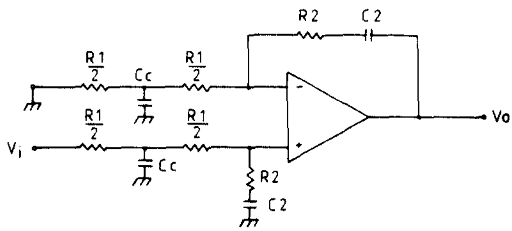

Fig. 7. Improved loop filter cicuit.

But if the cutoff frequency w_c is close to the natural frequency w_n in this circuit, pole is expected to be added and to produce even more overshoot.

Therefore, to avoid this damage, w_c must be at least 10 times more than w_n.

$$w_c = 4/(R1 * Cc) \tag{23}$$

$$w_c = 10 * Wn \tag{24}$$

$$C_c = 4/(Wc * R1) = 0.073 \text{ uF} \tag{25}$$

V. Computer Simulation

The used parameters for this simulation in case of 90 Mbps optical communication system are as following.

R1=1.5 KΩ
R2=10 KΩ
C2=0.047 uF
damping factor=0.8
Wn(natural freq.) =3,653 rad/sec

Kp=0.0593 V/rad
Kv=31,400 rad/V
p=1/2
Δf=60*90

The result of the simulation is shown in Table 1.

Table 1. Jitters along repeater chain.

N	Var. of alingment jitter	Var. of accumulated jitter
1	–.51766E + 01	–.51766E + 01
2	–.57350E + 01	–.24365E + 01
3	–.52186E + 01	–.59820E + 01
4	–.43574E + 01	.92713E + 00
5	–.33334E + 01	.23099E + 01
6	–.22106E + 01	.36234E + 01
7	–.10193E + 00	.49053E + 01
8	.22310E + 00	.61771E + 01
9	.15053E + 01	.74515E + 01
10	.28193E + 01	.87361E + 01
11	.41593E + 01	.10035E + 02
12	.55208E + 01	.11350E + 02
13	.69003E + 01	.12682E + 02
14	.82950E + 01	14031E + 02
15	.97027E + 01	.15395E + 02
16	.11122E + 01	16774E + 02
17	.12550E + 02	.18167E + 02
18	.13987E + 02	.19572E + 02
19	.15431E + 02	.20988E + 02
20	.16882E + 02	.22413E + 02
21	.18339E + 02	.23848E + 02

VI. Conclusion

D.L. Duttweiler derived the linear time-invariant model for PLL used as a timing extractor which was based on the study of B.L. Saltzberg.

In this paper we have improved the D.L. Duttweiler's model in the correct direction: Linear time-invariant model for PLL (Fig. 2. Fig. 3),z(k) (Eq. (11)), jitter power spectra and their variances in repeater chain (Eqs. (19), (20), (21), (22)). D.L. Duttweiler's the time-varying linear model for PLL was based upon Eq. (2). [1],[4] The correctly improved model is Fig. 2 in this paper.

The PLL as timing extractor of 90 Mbps optical communication system has been analyzed and used in this jitter analysis. Considering the worst case of repeater chain, the results have been shown in Table 1.

References

[1] D.L. Duttweiler, "The jitter performance of phase-locked loops extracting time from baseband data waveforms," B.S.T.J. vol. 55, No. 1, pp.37-58, Jan., 1976.

[2] E.D. Sunde, "Self-timing regenerative repeaters," B.S.T.J. vol. 36, no. 4, pp. 891-938, July, 1957.

[3] J.M. Manley, "The generation and accumulation of timing noise in PCM systems. -An experimentation and theoretical study," B.S.T.J, vol. 48, no. 3, pp.541-613, March, 1969.

[4] B.R. Saltzberg, "Timing recovery for synchronous binary data transmission," B.S.T.J, vol. 46, no. 3, pp.593-622, March, 1967.

[5] F.M. Gardner, Phaselock Techniques, 1979.

[6] 전자통신연구소 광통신 시스템 연구실 "90Mbps 광통신 시스템 연구보고"

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