論 文
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MOS 구조에서의 Avalanche Injection에 관한 연구

Characteristics of the Avalanche Injection on SiO_2 Layer in MOS Structures

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요 약

본 논문에서는 MOS 구조에 있어서 avalanche Injection 효과에 따른 산화막내의 전하축적 현상을 해석하기 위한 모델을 제시하였고 아울러 P형 Si 기판으로 제작된 MOS 커패시터의 C-V 특성 측정 등을 통하여 SiO_2 막내에서의 avalanche Injection 기구를 제시한 모델에 적용하여 고찰한 논문이다. 한편 avalanche Injection 기구를 고찰하는데 있어서 전하축적 현상과 산화막과 반도체 계면특성에 대하여서도 실험적인 결과를 토대로 정량적으로 해석하였다.

Abstract

A model is presented to explain charging phenomena into the oxide layer when a metal-oxide-silicon (MOS) capacitor is driven by a large amplitude and high frequency ac signal sufficient to produce avalanche injection in the silicon. During avalanche, minority carriers are injected. It is assumed that some of these minority carriers attain sufficient energy to surmount the potential barrier at the interface, and then inter the oxide.

Measurements of C-V curves are made for the MOS capacitor with p-type silicon substrates before and after avalanche injection. This paper studies how charging in the oxide and the interface depends on oxide properties. It is concluded that this charging effect is related to the presence of water in the oxide.

1. Introduction

Carriers can be injected into the SiO_2 layer of an MOS capacitor by avalanche injection.[1),2)] In many devices, avalanche injection into the thermally grown oxide occurs during normal operation. Control of injection as well as of subsequent trapping is important in limiting undesirable effects on device characteristics. The practical instances of avalanche injection into SiO_2 lie in very large scale integration. Very large scale integration incorporates MOSFETs with very small channel lengths. For n-channel MOSFETs, usually found in VLSI circuits, hot electrons are emitted from the silicon into the gate oxide when applied voltages are sufficiently large. Subsequent trapping of the electrons injected into the oxide can cause instability. However, avalanche injection can be used as a memory element in memory devices.

Injection of carriers into the oxide of an MOS capacitor by avalanche injection has been reported previously. The technique used is to drive the MOS capacitor with an ac signal of sufficiently large amplitude to induce avalanche breakdown in the p-type silicon substrate.

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The oxides are thermally grown on p-type silicon, and approximately 1000 Å thick. To study the dependence of charging effects on various oxide properties, three types of oxides will be grown on p-type silicon: (1) the dry oxygen-grown oxide, (2) the steam-grown oxide, and (3) the oxide grown in dry oxygen and subsequently exposed to water vapor.

In this paper, the effect of avalanche injection will be observed by the measurement of the C-V curves of a metal-oxide-silicon configuration.

In addition, we report a method for the determination of interface trap level density near midgap and oxide charge density before and after avalanche injection, which will enable us to observe the injection of electrons into silicon dioxide and trapping.

In Sec. 2, the principle of avalanche injection and the simple theories used in this paper will be introduced. In Sec. 3, the experimental techniques used will be described. While some of these are well known, sample preparation and details of the measurements are important to the unambiguous interpretation of the data. In Sec. 4, the experimental results will be described and discussed.

2. Theories

2.1 Physical Description of Avalanche Injection[3]

When the silicon bands are bent rapidly enough so that thermal equilibrium is not maintained, buildup of an inversion layer by thermal processes does not occur. Time constants for buildup of an inversion layer by thermal generation are usually between 0.1 and 1 sec. in silicon, therefore, if the frequencies of the large signal ac are in the MHz range, the silicon is driven into deep depletion. This condition is reached at time $t=t_1$ shown in Fig.1(b). The silicon band bending increases with further increase in field until avalanche breakdown initiated by thermally generated carriers occurs in the silicon.

The silicon remains in the avalanche breakdown condition during the time interval t_A shown in Fig.1(a). Electrons are excited from the valence band to the condition band of the silicon by the impact ionization.

Most of the electrons are excited to energies below the interfacial barrier height $\varnothing_B$ and these form an inversion layer. However, a few electrons are excited to energies above $\varnothing_B$. These electrons drift towards the Si-SiO_2 interface under the influence of the field in the silicon space charge region, obtain sufficient energies to overcome the potential barrier of about 3.13 eV shown in Fig.2, and then enter the silicon oxide conduction band. In the SiO_2 they probably soon drift towards the gate electrode under the influence of the field in the oxide. Avalanche breakdown in the silicon is extinguished when the oxide field passes its peak value. Thus, a pulse of electrons is injected into the oxide once per cycle during the interval t_A.

From the shifts in the C-V curves of the MOS capacitor found after avalanche injection, we can

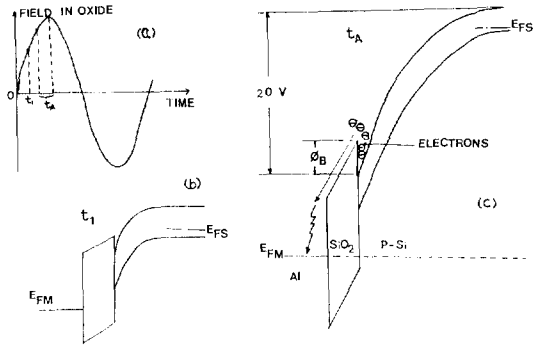

Fig. 1. The principles of avalanche injection: (a) shows one cycle of the oxide field produced by the external ac drive, (b) and (c) show the band bending during deep depletion and avalanche, respecively.

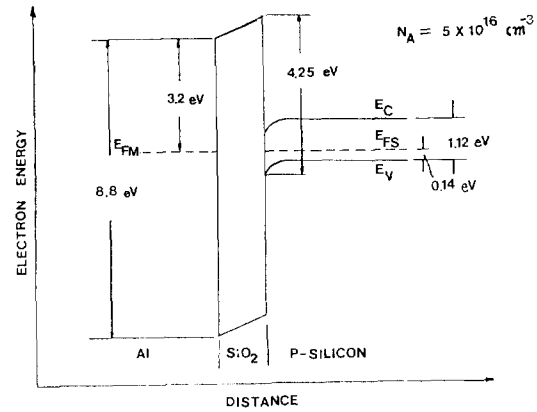

Fig. 2. Energy-band diagram of the MOS capacitor. The metal is aluminum and the silicon is p-type.

observe an increase in the fixed charge density in the oxide.

2.2 High Frequency Capacitance Method for Calculating Interface State Density near Midgap[4),5),6),7),8)]

From the capacitance measured as a function of gate bias, we determine interface trap level density as a function of energy in the silicon band gap. Because interface trap occupancy varies with gate bias, the slope of C-V curves measured at the MOS capacitor with interface traps is slower than that without interface traps.

In the MOS capacitor without interface traps, overall charge neutrality requires the change in gate charge to be balanced by a change in silicon surface charge Q_s. But, in the MOS capacitor with interface traps, a change in interface trap charge density Q_{it} also occurs with any change in band bending. Therefore, charge balance satisfies $Q_g+Q_{it}+Q_s=0$. Because the MOS capacitor with interface traps includes the additional change in charge density Q_{it}, the required change in Q_s is less. Thus the change in band bending is less in the MOS capacitor with interface traps than in the one without.

The equivalent circuit of the MOS capacitor is shown in Fig. 3. From Fig. 3,

$$C_{ox}(V_G-\psi_s) = -Q_{it}(\psi_s)-Q_s(\psi_s) \quad (1)$$

where C_{ox} = oxide capacitance per unit area (F/cm²), V_G = gate bias (V), ψ_s = band bending in the silicon surface (V), Q_{it} = interface trap charge per unit area (C/cm²), and Q_s = silicon surface charge per unit area (C/cm²). For an infinitesimal change in gate bias dV_G, Eq.(1) is replaced by

$$C_{ox}dV_G = (C_{ox}+C_{it}(\psi_s))d\psi_s \quad (2)$$

where $C_{it}(\psi_s) = -dQ_{it}/d\psi_s$ and $C_s(\psi_s) = -dQ_s/d\psi_s$ (3) are the interface trap and the silicon surface capacitance per unit area, respectively.

If band bendings do not place the Fermi level within a few kT/q of the band edges and if interface trap level densities do not vary rapidly over a few kT/q,

$$C_{it}(\psi_s)=q\,D_{it}(\phi_s) \quad (4)$$

where $\phi_s=\phi_B+\psi_s$.

$D_{it}(\varnothing_s)$ in Eq.(4) is the total density of interface trap

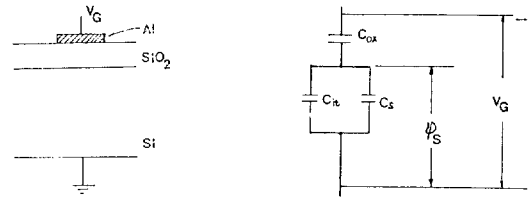

Fig. 3. Cross section of the MOS capacitor and its equivalent circuit.

levels at a position in the band-gap $\varnothing_s$ from the intrinsic level at the silicon surface.

Because interface traps do not respond to the high frequency ac gate voltage, they contribute no capacitance to the C-V curve. Therefore, regardless of interface trap level density, the high frequency capacitance of an MOS capacitor will be the same as that of an ideal one without interface traps and given by

$$C_{HF}=\frac{C_s\cdot C_{ox}}{C_s+C_{ox}} \quad (5)$$

However, as interface traps do follow changes in gate bias, they cause the high frequency C-V curve to stretch out along the gate bias axis because interface trap occupancy must be changed in addition to charging depletion layer charge.

However, measured C_{HF} will be the same as the ideal if band bending is the same.

Knowing ψ_s corresponding to a given C_{HF} in the ideal MOS capacitor and measuring V_G corresponding to the same C_{HF} in the real MOS capacitor, we can construct a ψ_s versus V_G curve for the MOS capacitor with interface traps. To obtain this ψ_s versus V_G relationship, we first find how C_s varies with ψ_s (band bending). For a given doping profile, C_s is a known function of band bending. If biases in inversion are avoided, where the frequency response of the inversion layer introduces complications, C_s is frequency independent and easily calculated. Then $C_{it}(\psi_s)$ can be determinded from Eq.(2) as

$$C_{it}(\psi_s)=C_{ox}((d\psi_s/dv_G)^{-1}-1)-C_s(\psi_s). \quad (6)$$

$Dit(\phi_s)$ (cm⁻² eV⁻¹) is calculated from Eq. (4), and $C_s(\psi_s)$ in Eq. (6) will be described in Appendix A.

2.3 Method for Measuring the Change of Oxide Charge from the Voltage Shift of a C-V Curve[9)-13)]

Avalanche injection commonly effects on oxide charge. We start by calculating the effect of oxide charge on the C-V curve. This charge induces an image charge in the silicon surface. The flatband voltage shift between the C-V curve before and after avalanche injection is a measure of the trapped oxide charge density.

To obtain flatband voltage from a measured C-V curve, the theoretical curve is calculated for a device without oxide charges or work function difference,but with the same oxide thickness and doping profile as the experimental device. This C-V curve is plotted on the same axes as the measured C-V curve, and separation of the two C-V curve is V_{FB}.

In summary, V_{FB} is given by

$$V_{FB}=W_{ms}-V_N-C_{ox}^{-1}(Q_0+Q_{it}(o)+Q_S(o)) \quad (7)$$

where W_{ms} = work function difference,

Q_o = oxide charge per unit area near the $Si-SiO_2$ interface,

$Q_{it}(O)$ = interface trap charge per unit area at $\psi_s=O$,

$Q_s(O)$ = silicon surface charge per unit area at $\psi_s=O$,

C_{ox} = oxide capacitance per unit area, and

V_N = voltage shift caused by the nonuniform doping profile.

The terms changed after avalanche injection are Q_o and $Q_{it}(O)$ of Eq.(7). By the change of Q_o and $Q_{it}(o)$, flatband voltage is shifted, and this is observed by measuring the C-V curves.

2.4 Measurement of the Oxide Thickness without Knowing the Area of the Gate Contact[14)]

E.H. Nicollian et al. suggested that oxide thickness was calculated from a plot of $(C_{ox}/C_{HF})^2$ vs.voltage, where C_{ox} is oxide capacitance and C_{HF} is the high frequency capacitance at the gate voltage V_G. The slope of the linear portion of such a curve depends on oxide thickness and doping density according to

$$t_{ox}=\left(\frac{2\varepsilon_{ox}}{q\varepsilon_s}\right)^{\frac{1}{2}}(S\cdot N_A)^{-\frac{1}{2}}=1.17\times10^3(S\cdot N_A)^{-\frac{1}{2}} \quad (8)$$

where t_{ox} is oxide thickness, ε_{ox} and ε_s are the oxide and silicon permittivities, respectively, N_A is the ionized acceptor density cm^{-3}, and S is the slope of the linear portion of $(C_{ox}/C_{HF})^2$ vs.voltage in units of $(V)^{-1}$.

3. Sample Preparation and Measuring Technique

3.1 Sample Preparation

A MOS capactor is made to observe the negative charging effects into thermally grown SiO_2 layer by avalanche injection. We briefly consider 1) a silicon substrate, 2) wafer cleaning, and 3) oxidation processes.

1) Silicon Substrate (p-type, doping density: $5\times10^{16}cm^{-3}$, (100))

We confine attention to electron injection from p-type silicon because electron injection is much easier to control than hole trapping in the oxide. For an n-type substrate, avalanche results in hole injection into the SiO_2. In this case, one major problem is that injected charge is not only hole. That is, besides the flow of holes from the silicon to the gate, a large electron injection occurs from the gate to the silicon. Further, electron injection can occur by field emission from the edges of the gate electrode due to the sharpness of the gate edge.

The doping density of the substrate used is in the range of $5\times10^{16}cm^{-3}$. Avalanche injection experiments are practical over only a limited range of silicon doping density. For sufficiently low doping density, edge breakdown is expected, and dielectric breakdown can occur before the electric field reaches avalanche breakdown. While, for sufficiently high doping density, interband tunneling rather than avalanche breakdown occurs in the silicon.

(100)-oriented substrates are used because the interface trap density of (100) is less than that of (111).

2) Wafer Cleaning[15)]

Wafer cleaning before, during, and after oxidation is perhaps the most important requirement for growing high quality oxides. Impurities present on the silicon surface prior to oxidation or during the oxide growth itself influence the homogeneity of the film and the interface electrical properties.

A preoxidation cleaning procedure is:

(1) Clean ultrasonically in trichloreethylene

(2) Rinse in acetone

(3) Heat at 95°C in a solution of equal parts (v/v) of H_2O_2(6%), NH_4OH and DI water for 30 minutes

(4) Rinse in DI water

(5) Immerse in aqua regia (1 minute)

(6) Rinse in DI water

(7) Immerse in HF (30 minutes)

(8) Rinse in DI water

(9) Repeat steps 5 through 8 three times and finally flush thoroughly in DI water after the final aqua regia washing

(10) Dry the water in hot clean gas flow.

DI water of high purity (5 megohm-cm) is used for this cleaning.

3) Oxidation Processes[16),17)]

In order to observe the effect of avalanche injection for different oxide properties, we prepare(a) the oxide grown thermally in dry oxygen, (b) the oxide grown thermally by steam oxidation, and(c) the oxide grown thermally in dry oxygen and subsequently exposed to water, but, in this case, water must not reach the silicon oxide interface.

Experimental systems for above oxidation processes are shown in Fig.4, Fig.5, and Fig.6, respectively.

Oxide thicknesses obtained in these processes are calculated from Deal and Grove method.[18)20)]

The oxide thickness of the samples should be in the range of 1000-1100 Å to avoid tunneling, dielectric breakdown and edge breakdown.

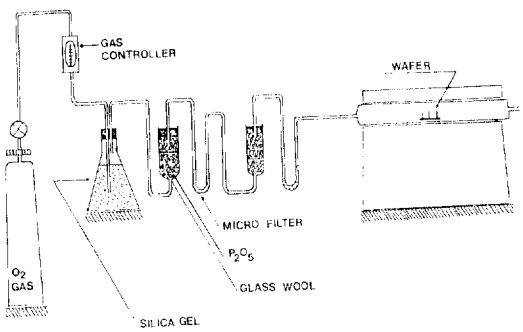

Fig. 4. Experimental system for dry oxidation

Experimental procedures for the case of (c) are as follows.

The samples are prepared by diffusing water into the SiO_2 grown by the procedure described in Section (a). Before gate electrodes are evaporated on the samples, it is held at diffusion temperature (180°C) in the furnace for a given time (5min) while a stream of nitrogen gas saturated with water vapor flows over it. Nitrogen saturated with water vapor is produced by bubbling nitrogen gas through a water vessel. The total pressure of nitrogen plus water vapor is kept just slightly above atmospheric pressure. Doing this prevents back flow of air into the system.

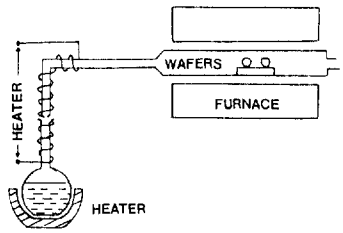

Fig. 5. Experimental system for steam oxidation[19)]

To obseve the dependence of charging effects on water temperature in the water vessel, the samples are prepared in the range of 50 to 90°C.

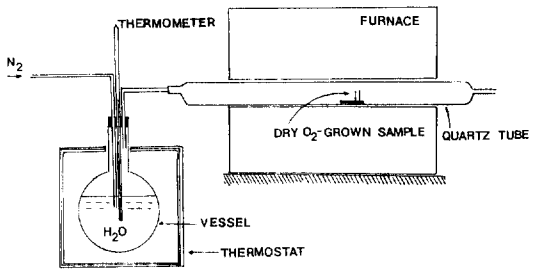

Fig. 6. Experimental system for diffusing water into oxide

3.2 Measuring Technique

In order to observe the trapping and charging effect into the oxide by avalanche injection, we measure the C-V curves. Fig. 7 shows a schematic diagram of a Wafer Analyzer used to measure the high frequency C-V curve of the MOS capacitor.

First, the MOS capacitor is heated for 10 min at 200°C with −15V applied to the gate in order for all of the available sodium ions[21)] to drift completely across the oxide. Then we measure the C-V curve for the MOS

capacitor before avalanche injection.

The large signal ac (frequency 1.5MHz, amplitude 20V) is applied to the samples with a RF generator for 10 min and then we measure the C-V curve with the Wafer Analyzer.

Each measurement described above is made for three types of oxides, that is, the oxide grown in dry oxygen, the oxide grown by steam oxidation, and the oxide which is first grown in dry oxygen and then exposed to water vapor.

We observe the change of flatband voltage shift and the slope of the C-V curve for each sample.

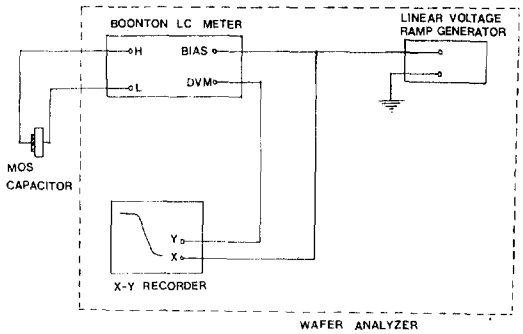

Fig. 7. Schematic diagram of the water analyzer.

4. Experimental Results and Discussion

As described in Sec.3.2, measurements of the C-V curves of the MOS capacitor for three types of the oxides were made before and after avalanche injection.

Fig. 8, 9 and 10 indicate the C-V curves measured for the oxide grown in dry oxygen, the steam grown oxide, and the oxide grown in dry oxygen and subsequently exposed to water vapor, respectively, before and after avalanche injection.

Generally, electrons are injected when the substrate is p-type and holes when the substrate is n-type. If the sufficiently large signal ac is applied to the gate electrode of the MOS capacitor, electrons for p-type substrates or holes for n-type are injected into the thermally grown oxide by avalanche injection, and a charging effect in the oxide is accompanied.

Experimental results from a MOS capacitor with p-type silicon substrates are a negative oxide charging effect. However, as shown in Fig. 8, 9 and 10, it has been observed that the changes of the C-V curves measured for each type of the oxide after avalanche injection are different. That is, for dry oxygen-grown SiO_2, any increase in interface trap level density and oxide charge density has been scarcely observed after injection, as shown in Fig. 8. However, for steam-grown SiO_2, an increase in the oxide charge density near the $Si\text{-}SiO_2$ interface has been observed (through the shifts to the positive gate voltage axis in the C-V curves found after avalanche injection). In addition, an increase in interface trap level density has been also observed (through the slow slope of the C-V curve after injection). Interface trap level density near midgap calculated by the method described in Sec. 2.3 has increased from $4\times10^{11}cm^{-2}\,eV^{-1}$ to $9\times10^{11}cm^{-2}eV^{-1}$. For the oxide grown in dry oxygen and subsequently exposed to water vapor, a voltage shift of the C-V curve without altering its shape has been observed after avalanche injection, as shown in Fig. 10.

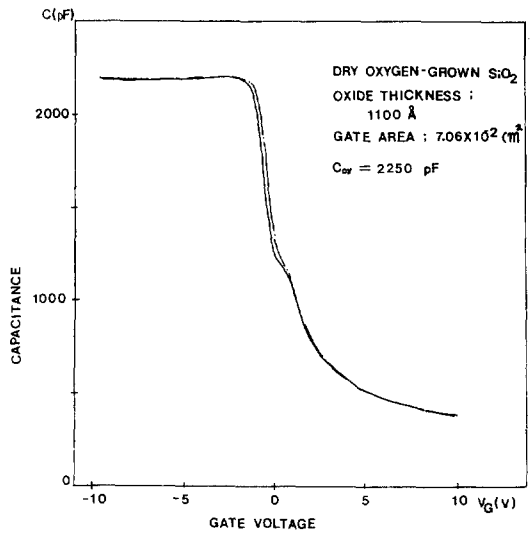

Fig. 8. C-V curves measured for a dry oxygen-grown oxide before and after avalanche injection. Curve a is before avalanche injection and curve b is after injection.

For the results observed in a steam-grown oxide and a dry oxygen grown oxide after avalanche injection, the charging effect appears to be related to the presence of water in the oxide. Holmberg et al.[22] working in similar temperature and hydration pressure ranges

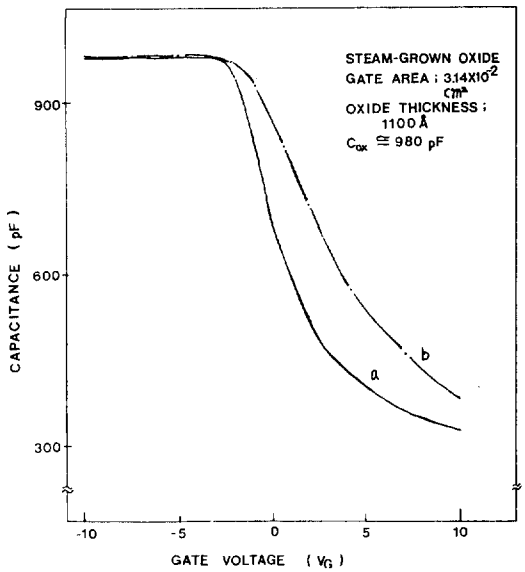

Fig. 9. C-V curve measured for a steam-grown oxide before and after avalanche injection. curves a and b are before and after avalanche injection, respectively.

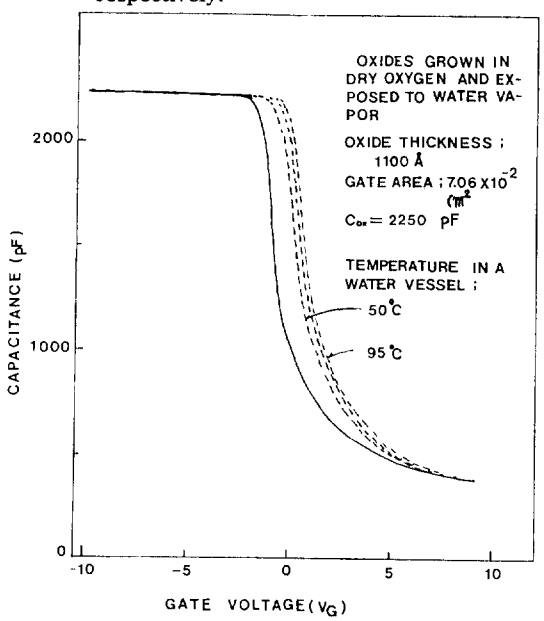

Fig. 10. C-V curves measured for the oxide grown in dry oxygen and subsequently exposed to water vapor before and after avalanche injection with water temperature in a vessel as a parameter.

found that the concentration of hydrogen in the oxide varied as the partial pressure of water $(P_{H_2O})^{1/2}$ which means that the water molecules dissociate into two fragments on intering the oxide. Schmidt suggested a possible mechanism to explain the negative charging effect. It involves chemical decomposition of defect centers in the oxide. These defects normally have no net charge, but hydrogen ions are incorporated in them. When electrons are injected, some of them are captured by the hydrogen ions, producing neutral hydrogen. The neutral hydrogen diffuses rapidly to the interface, and negative charge is left behind in the defect. That is, negative charge is accumulated in the oxide. From the fact that is explained above, there can be little doubt that negative oxide charge produced in injecting electrons into the oxide is caused by electron capture at a water related center in the oxide.

The negative charging effect is probably not the usual electronic trapping involving a fixed density of immobile traps. This is suggested by the fact that (1) this oxide is not discharged by exposure to intense visible and ultraviolet light regardless of an accelerating field applied to a gate electrode and (2) the activation energy of 0.35 eV is too low to permit traps to remain charged when fields of several million voltages per cm are applied across the oxide by the ac drive.

Fig. 10 shows the dependence of flatband voltage shift ΔV_{FB} on diffused water temperature in a water vessel shown in Fig. 6. It has been obseved that ΔV_{FB}

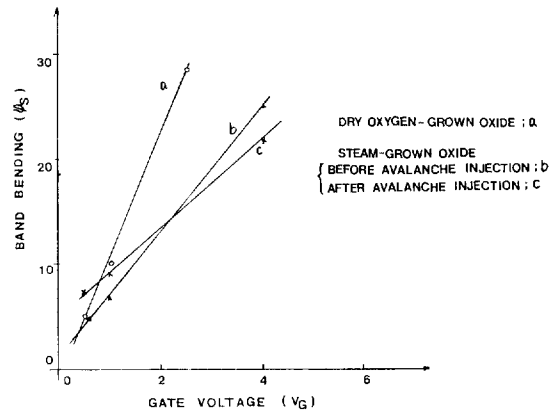

Fig. 11. ψ_s vs V_G curves for various C-V curves. Curve a is for a dry oxide (Fig. 8), curve b is for a steam grown oxide before avalanche injection (curve a in Fig. 9), and curve c is for a steam grown oxide after avalanche injection (curve b in Fig. 9).

increases with increasing water temperature, that is, the amount of negative oxide charge produced by a given flow of injected electrons increases with the amount of water vapor diffused into the oxide.

Fig. 11. shows a set of ψ_s vs V_G curves plotted from the C-V curves shown in Fig. 8, 9 and 10, which need for determining interface trap level density D_{it} near midgap. The values of the slope of ψ_s vs. V_G curves are substituted into Eq.6, so that D_{it} is found. Curve a is a ψ_s vs V_G curve otained for dry oxygen-grown SiO_2. In this case, the interface trap level densities found were in the range of about $1\times10^{11}cm^{-2}eV^{-1}$. Curve b, and c are the ψ_s vs V_G curves for the oxide grown in dry oxygen and subsequently exposed to water vapor before and after avalanche injection, respectively. As described above, interface trap level densities has increased from $4\times10^{11}cm^{-2}$ to $9\times10^{11}cm^{-2}eV^{-1}$.

5. Conclusions

Avalanche injection has commonly effects on oxide charge density and interface trap level density. When a substrate is p-type, electrons are injected, so that a negative oxide charging effect occurs.

Experimental results are that a charging effect in the oxide and interface depends on oxide properties, that is, (1) no charging effect in the dry oxygen-grown oxide occurs, (2) a charging effect in the steam grown oxide occurs in the oxide and the interface, and (3) one in the oxide grown in dry oxygen and subsequently exposed to water vapor occurs in the oxide, but not the interface.

It is clear that negative charging produced by injecting electrons into the thermally grown oxide is caused by electron capture at a water related center in the oxide.

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Appendix A

Method for Calculating C_s (ψ_s)

Energy band diagram of the MOS capacitor for p-type silicon is shown in Fig. 12.

By definition, the silicon surface capacitance is given by

$$C_s = \varepsilon_s \frac{\delta}{\delta V_s}\left(\frac{dv}{dx}\right)_{x=0} \qquad (A1)$$

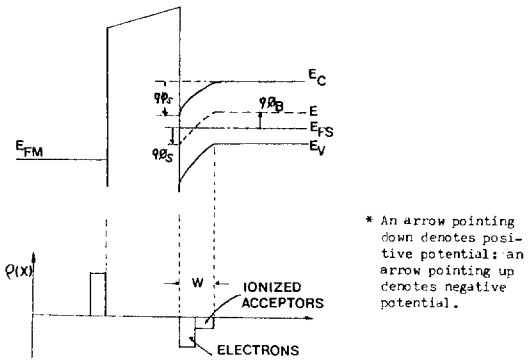

Fig. 12. Energy band diagram of the MOS capacitor for p-type.

where $v(x,t)=(kT/q)\ \psi(x,t)$.

The Poisson equation for p-type is used to find the dimensionless electric field $(dv/dx)_{x=0}$ at the silicon surface. $(dv/dx)_{x=0}$ for $v_s>0$ is given by

$$\left.\frac{dv}{dx}\right|_{x=0}=2^{\frac{1}{2}}\lambda_p^{-1}\{v_s+\exp(-v_s)-1+\exp(u_B-u_{Fn})\cdot[(\exp(v_s)-1)]\}^{\frac{1}{2}} \quad (A2)$$
$$=F(v_s,\ u_{Fn},\ u_B)\,\lambda_p^{-1}$$

Therefore, Eq.(A1) becomes (for $v_s>0$)

$$C_s=C_{FBS}\{1-\exp(-v_s)+(\frac{n_i}{N_A})^2[(\exp(v_s)-1)(1-\frac{\delta u_{Fn}}{\delta v_s})+1]\}\ F^{-1}(v_s,\ u_B,\ u_B) \quad (A3)$$

where $C_{FBS}=\frac{\varepsilon_s}{\lambda_p}$, $\lambda_p=(\frac{\varepsilon_s kT}{q^2N_A})^{\frac{1}{2}}$, and $u_{Fn}=u_B+\delta u_{Fn}=\frac{E_{Fn}-E_i}{kT}$.

In obtaining Eq.(A3), the small-signal approximation has been made that $U_{Fn}\cong U_B$, and the relation $\delta/\delta v_s(\exp(u_{Fn}))=(\delta u_{Fn}\gg\delta v_s)\exp(u_{Fn})$ has been used.

Two effects must be considered in obaining the high frequency inversion capacitance. First, the total number of minority carriers is fixed by the quiescent gate bias and does not change in response to ac gate voltage. Second, minority carriers can move spatially at the silicon surface in response to the high frequency gate voltage. The quasi-Fermi level moves up and down in each cycle to adjust the level of occupancy in the conduction band so that the net electron density per unit area always is fixed, independent of time, while the volume density varies. The ac electron quasi-Fermi level E_{Fn} is considered spatially uniform within the inversion layer where the electron density is significant.

We introduce the small-signal analysis defined by

$$\frac{\delta u_{Fn}}{\delta v_s}=\frac{1}{1+\Delta} \quad (A4)$$

where Δ is a fraction taking into account the constancy of inversion layer charge and its spatial redistribution. When the MOS capacitor is in strong inversion, $\delta u_{Fn}/\delta v_s\cong 1$. Now we can rewrite Eq.(A3) in terms of Δ, and obtain

$$C_s=2C_{FBS}\{1-\exp(-v_{so},)+(\frac{n_i}{N_A})^2[(\exp(v_{so})-1)\frac{\Delta}{1+\Delta}+1]\}\ F^{-1}(v_{so},\ u_B) \quad (A5)$$

where v_{so} is the band bending at the surface established by the gate bias. Eq.(A5) is an accurate expression for the high frequency capacitance.

In the range of $v_{so}\leqslant 2\,u_B$, the redistribution effect is negligible because minority carrier concentration has become small compared to acceptor concentration. Therefore, minority carrier terms in Eq.(A5) can be neglected so that Eq.(A5) becomes (for $0<v_{so}\leqslant 2\,u_B$)

$$C_s=C_{FBS}\{1-\exp(-v_{so})\}\ F^{-1}(v_{so},\ u_B)$$
where $F(v_{so},\ u_B)$ (A6)
$$=2^{\frac{1}{2}}(v_{so}-1+\exp(-v_{so}))^{\frac{1}{2}}$$ for p-type.

For $v_{so}\geqslant u_B$, minority carrier concentration is comparable to or higher than N_A and redistribution becomes important. Therefore, $\delta u_{Fn}\gg\delta v_{so}$ is close to unity so that $\Delta\ll 1$, and Eq.(A5) becomes (for $v_{so}\geqslant 2\,u_B$)

$$C_s=C_{FBS}\{1-\exp(-v_{so})+(\frac{n_i}{N_A})^2[(\exp(v_{so})1)\Delta+1]\}\ F^{-1}(v_{so},\ u_B) \quad (A7)$$

for p-type.