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# Optimization of PSG Flowing and Metallization for Step Coverage Improvement

# (스텝 커버리지를 위한 PSG와 金屬處理 工程 條件의 改善)

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要 約

LSI나 VLSI 소자의 제조 공정중 금속막이 기존의 스텝 커버리지를 좋게 하는 것은 매우 중요한 일이다. 본 연구에서 얻어진 방법은 8.0~8.6 wt.%의 인을 포함하는 PCG를 증기(steam) 분위기의 950℃에서 30분간 열처리한 후 250℃에서 1 um의 알루미늄을 증착하는 것이다.

**Abstract**

One significant problem which arises during the fabrication of LSI and/or VLSI is how to make a good step coverage for aluminum. One way developed in this study is to flow PSG containing 8.0 wt.% – 8.6 wt.% of phosphorus at 950°C for 30 minutes in steam and to depo3it aluminum of 1 um thickness at 250°C.

## I. Introduction

Phosphosilicate glass (PSG) annealing or flowing is one method to improve step coverage for silicon-gate MOS integrated circuits, where the steps are formed by poly-silicon interconnect, field oxide and contact holes.

A smooth step contour can be obtained by annealing the glass with excess phosphorus at relatively low temperature. It was found that aluminum on highly doped PSG, however, is apt to suffer corrosion. On the contrary, if the glass contains less phosphorus, the junction formed already may become too deep to be relevant to a device during high temperature annealing process.

Heating the substrate during metal deposition is another technique to improve the coverage of metal films by increasing the mobility of metal species.[1]

## II. Experiments

Oxide steps of 1.0 um and 0.6 um were constructed on p-type, (100) and 3-inch wafers with the resistivity of 15 Ω-cm~20Ω-cm. PSG films containing 7.3 wt.% to 9.0 wt.% of phosphorus were deposited on the oxide steps with a CVD system. The thickness of the PSG films was varied from 0.6 um to 1.0 um with the uniformity of ±5%. The measurements of phosphorus concentrations were referenced to diffusion and etching techni-

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ques.[2,3]

Flowing was carried out in the temperature range of 900°C and 1000°C in a steam ambient to reduce the flow time[4] and then contacts were opened. Pure aluminum of 1.0 um or 1.5 um was deposited on the PSG step with an E-gun. The deposition rate and vacuum level were 20 Å/sec and $3\times10^{-6}$ Torr respectively. The substrate temperature was varied from 150°C to 250°C.

We applied the standard silicon-gate NMOS process to define steps and metal lines. The mask layers are active, polysilicon, contact and metal masks.[5]

A scanning electron microscope (SEM) was used to observe the step contour. Electrical evaluation of coverage was performed by measuring resistance at room temperature and burn-out current of the metal lines. When DC voltage applied to both ends of resistor is increased gradually, the metal line will be burnt out to give a burn-out current.

A problem in comparing the measured data is different extents of overetching of metal lines from wafer to wafer and from chip to chip. The data were normalized as follows.

Fig. 1 shows two kinds of metal patterns. (A) is running over steps and (B) is running on a plane. The extent of overtching was assumed to be the same within a chip. The ideal resistances of the metal pattern (A) and (B), if without overetching and without steps under metal, can be expressed as

$$R_A = R_s \cdot L_A/S \tag{1}$$

$$R_B = R_s \cdot L_B/S \tag{2}$$

Rs is the sheet resistance of metal films. When S is reduced to S' by overetching and there are steps under metal lines of pattern(A), the measured resistances are given by

$$R'_A = R_s \cdot L_A/S' + R'_{sc} \tag{3}$$

$$R'_B = R_s \cdot L_B/S' \tag{4}$$

Where $R'_{sc}$ is the increased resistance due to [illegible] and narrowing of metal lines formed [illegible] shown in Photo 1. From the Eq.(2) and Eq.(4)

$$R_B/R'_B = S'/S \tag{5}$$

By applying Eq.(5) to Eq.(3) to obtain the following equation

$$\begin{aligned} R'_A \cdot R_B/R'_B &= R_S \cdot L_A/S + R'_{sc} \cdot S'/S \\ &= R_A + R'_{sc} \cdot S'/S \\ &\equiv R_n \end{aligned} \tag{6}$$

Where $R_B$ is given and $R'_A$ and $R'_B$ are the measured values. The normalized resistance, $R_n$, is consist of the ideal resistance term and the normalized resistance term which comes from the poor coverage and defects. Normalizing the burn-out current in same way, one can obtain the following expression.

$$I_n \equiv I'_A \cdot S/S' = I'_A \cdot R'_B/R_B \tag{7}$$

Where $I'_A$ is the measured burn-out current of the pattern (A). All electrical values plotted were normalized through the relations.

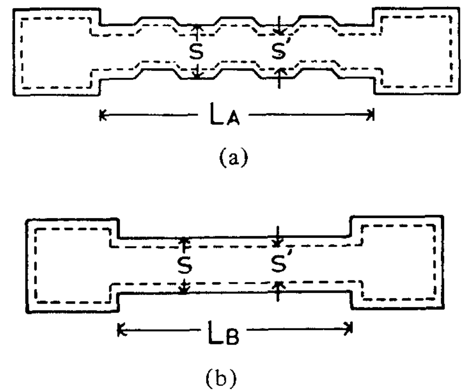


**Fig. 1.** Schematic demonstration of overetching of the step pattern (A) and the reference pattern without steps (B). $L_A$ is the horizontal distance in which step heights are not included.

### III. Result and Discussion

When 1.5 um pure aluminum was deposited on the unflown 1.0 um steps, there appeared

**Photo 1.** Defects appearing in metal films over unflown steps. Microcrack, concave etch defect and capillary tunnel are shown by arrows.

some structural defects such as capillary tunnels, microcracks and etching defects of concaves as shown in Photo 1.

The vertical or retrograding steps shadow the bottom edge area and prevent aluminum species from arriving there during deposition. This geometric shadow effect is inferred to create the capillary tunnels which had been concluded to be a cause of op[illegible]circuits.[1] The microcracks come also from shadow effect. The geometric shadowing of the steep wall and self-shadowing of growing aluminum create microcracks at the top edge area to generate very thin metal films. The thinning effect makes large concaves after isotropic metal etching. Conclusively, all these defects originate from the step contour of steepness and contribute to diminish the metal line width locally at step edges.

*1. Effects of Substrate Heating and Metal Thickness*

The formability of microcracks can be controlled by adjusting the ratio of metal film thickness(t) to step height(h), i.e. t/h. The greater the ratio is, in the case of $t/h > 1$, the more easily defects form.[6] Aluminum films of 1.0 um over 1.0 um steps ($t/h = 1.0$) are giving lower resistances and higher burn-out currents than those of 1.5 um over the steps with same height ($t/h = 1.5$) as shown in Fig. 2. The effect can be identified by comparing Photo 2 with Photo 3. The coverage ratio defined by the ratio of metal film thickness at the top edge to that at the normal plane was much increased by only reducing the metal films thickness. Large coverage ratio gives more uniform etching.

The step coverage was also improved by increasing the substrate temperature during metal formation. As shown in Photo 2, higher substrate temperature made the crack-tips blunt. The effects are also revealed in resistance data shown in Fig. 2. The effect was much greater on the unflown steps and, however, not very noticeable in the steps flown at 950°C for 30 minutes.

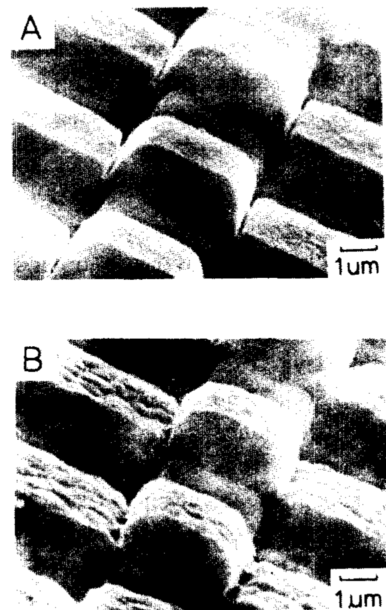


**Photo 2.** Morphology of step coverage when PSG film of 8.6 wt.% phosphorus is flown at 920°C for 30 minutes and 1.5 um aluminum is deposited at (A) 150°C and (B) 250°C.

*2. Optimization of the PSG Flowing*

As shown in Fig. 2, the effect of substrate heating becomes not very significant when PSG flows at over 950°C. So a suitable flowing treatment of the PSG films is prerequisite.

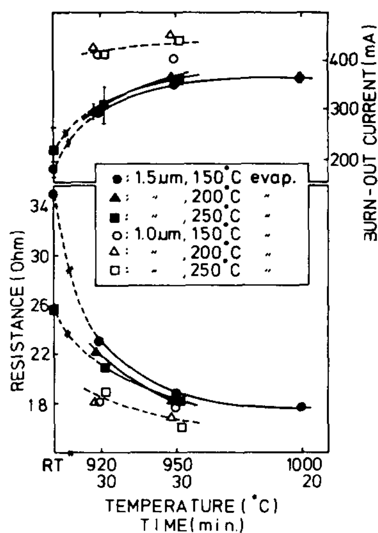


Fig. 2. Electrical evaluation of coverage on 1.0 um steps. Effects of metal thickness, substrate and flowing temperature are shown.

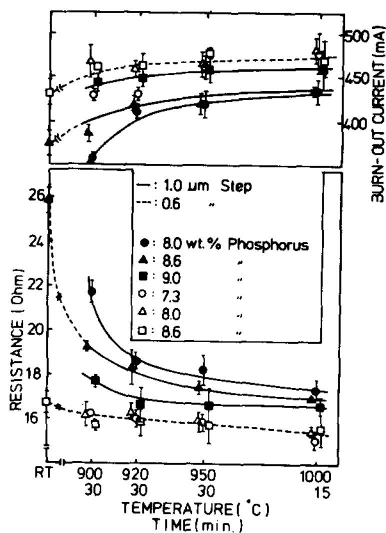


Fig. 3. Effects of phosphorus concentration and flowing temperature are shown. Aluminum was deposited at 250°C with 1.0 um thickness.

Both of electrical evaluation and SEM investigations were conducted in order to establish an optimum flowing condition.

The photographs of the SEM show the acceptable layer can be obtained by flowing 8.6 wt.% PSG at 950°C for 30 minutes. The normalized resistance value and the coverage ratio measured from the treated oxide were 17.5 Ω and 60% repectively. It was checked by SEM that samples having resistance values less than 18 Ω among the samples in Fig. 3 had nearly equal coverage ratios. The slope of the step wall was less than 60° as shown in Photo 3-(A).

A problem arising from the process is short between the metal and the underlying polysilicon during the fabrication of SG-MOS devices. It comes from exposing the silicon step edges out of the PSG layers as a result of over flowing. The thickness of 1.0 um of the PSG film was thought to be thick enough to avoid the short-circuiting after flowing as shown in Photo 3-(B).

When the step height for polysilicon in a SG-MOS process is about 0.6 um, step coverage

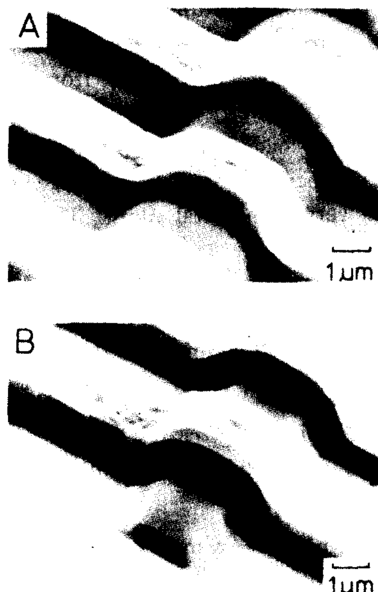


**Photo 3.** (a) Morphology of step coverage when PSG film of 8.6 wt.% phosphorus is flown at 950°C for 30 minutes and 1.0 μm aluminum is deposited at 250°C.
(b) Photo taken after HF dip of sample A to remove PSG layer.

was also investigated after flowing 0.6 um PSG films over the steps. As shown in Fig. 3, the electrical measurements show somewhat different tendency with the variations of phosphorus concentration. There was only slight coverage improvement with increasing the flowing temperature. The step height of 0.6 um is inferred to be not so high enough to cause severe coverage problem. The coverage ratio of the unflown sample, as shown in Photo 4-(A), is approaching 50%. But the flowing treatments at 950°C for 30 minutes, 900°C for 30 minutes and 1000°C for 15 minutes for the PSG films containing 8.0, 8.6 and 7.3 wt.% phosphorus respectively improved the coverage ratio upto 70% as shown in Photo 4-(B). The flowing treatments are thought to remove the coverage problem for 0.6 um steps almost entirely.

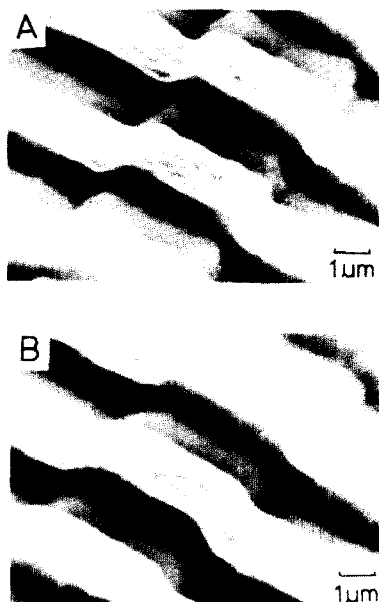


**Photo 4.** Morphology of step coverage.
(a) Before flowing of PSG film deposited on 0.6 um step.
(b) After flowing of the PSG film of 8.0 wt.% phosphorus at 950°C for 30 minutes.

## IV. Conclusion

General effects of the metal substrate temperature, metal to step height ratio and the PSG layer flowing have been studied. Substrate temperature of 250°C and lowering the ratio of t/h by 1.0 could improve the step coverage.

We must dope phosphorus upto 8.0-8.6 wt.% to obtain suitable step coverage after flowing oxide. The PSG films containing 8.6 wt.% phosphorus need to be flown at 950°C for 30 minutes in a steam ambient for the acceptable coverage of 1.0 um step height. In the case of lower step height, 0.6 um, the fabrication of the devices without flowing treatments could be possible. There is almost no coverage problems for the flown 8.0 wt.% PSG films at 950°C for 30 minutes in a steam ambient.

## References

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