비정현 계통 전압하에서 단상 인버터의 PLL 성능 개선 방법

A Method to Improve the Performance of Phase-Locked Loop (PLL) for a Single-Phase Inverter Under the Non-Sinusoidal Grid Voltage Conditions

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ABSTRACT

The Phase-Locked Loop (PLL) is widely used in grid-tie inverter applications to achieve the synchronization between the inverter and the grid. However, its performance is deteriorated when the grid voltage is not pure sinusoidal due to the harmonics and the frequency deviation. Therefore it is important to design a high performance phase-locked loop (PLL) for the single phase inverter applications to guarantee the quality of the inverter output. In this paper a simple method to improve the performance of the PLL for the single phase inverter is proposed. The proposed PLL is able to accurately estimate the fundamental frequency component of the grid voltage even in the presence of harmonic components. In additional its transient response is fast enough to track a change in grid voltage within two cycles of the fundamental frequency. The effectiveness of the proposed PLL is confirmed through the PSIM simulation and experiments.

Index Terms – Synchronous frame PLL (SRF-PLL), phase lock loop (PLL), synchronization, single phase grid connected converter, filter.

1. Introduction

A phase-locked loop (PLL) is a technique with three distinct parts, i.e., a phase detector, a loop filter (LF), and a voltage-controlled oscillator, that adjusts the phase of its output signal to follow the phase of its input. The accurate detection of the frequency and phase angle made PLL very popular for synchronization and control purposes in grid-connected applications [1]. In single phase system there is less information than three phase system regarding grid condition, so more advance techniques are required in order to generate the orthogonal signal [2]. The most commonly used methods are all pass filter (APF) and second order generalized integrator (SOGI). The SOGI and APF SRF-PLL can provide a satisfactory performance when grid voltage is sinusoidal but their performance is degraded under non-sinusoidal grid voltage. In order to extract the accurate phase and frequency component of grid voltage under non-sinusoidal and sinusoidal condition the SOGI based low pass filter (LPF) SRF-PLL is proposed in this paper. The proposed PLL can estimate the frequency and phase more accurately and transient response is fast enough to track the grid voltage with in two cycles.

The paper is organized as follows: An overview of APF SRF-PLL under sinusoidal and non-sinusoidal grid voltage in section 2. In section 3 SOGI SRF-PLL under sinusoidal and non-sinusoidal grid voltage is discussed. In section 4 discuss about purposed SOGI LPF SRF-PLL under sinusoidal and non-sinusoidal grid voltage. In section 5 simulation and experimental results are evaluated and in the end conclusion is discussed in section 6.

2. APF SRF-PLL Under Sinusoidal and Non-Sinusoidal Grid Voltage

In APF SRF-PLL system, the virtual two-phase voltages V_α and V_β can be obtained from the measured grid voltage V_g by using digital APF then park transformation is applied on these signals as Shown in Fig.1, where $V_\alpha = V_g \mathrm{Cos}\Theta$ and $V_\beta = V_g \mathrm{Sin}\Theta$. The Laplace transform of APF can be expressed as Eq. (1)

$$G_{APF}(s) = \frac{s-\omega_A}{s+\omega_A} \qquad (1)$$

Where ω_A is the cut-off angular frequency. Once the orthogonal signal has been generated, the park transformation is used to detect the v_d, v_q components on the rotating frame. Then these signals are fed to the LF that control the VCO of the PLL. Under the sinusoidal grid voltage condition the performance of APF SRF-PLL is good but it causes an oscillation in frequency under the non-sinusoidal grid voltage since it cannot generate the estimated theta Θ_{out} accurately. The frequency responses in both cases are shown in Fig.2 and the Bode plot of APF is also shown in Fig.3.

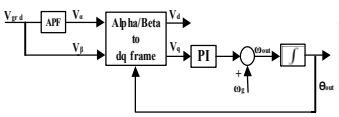


Figure 1 Schematic diagram of APF PLL

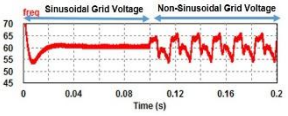


Figure 2 Frequency response of APF PLL

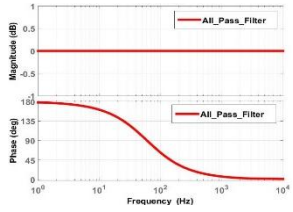


Figure 3 Bode plot response of APF SRF PLL

3. SOGI SRF-PLL Under Sinusoidal and Non-Sinusoidal Grid Voltage Conditions

Fig.4 shows the schematic diagram of single phase SOGI SRF-PLL, SOGI generates virtual signals V_α with the same phase and magnitude as the fundamental of the input signal and V_β with a phase shift of 90 degree. The closed-loop transfer function (TF) of the SOGI based quadrature signal generator (QSG) can be expressed as Eq. (2) and Eq. (3)

$$H_d(s) = \frac{v'}{v}(s) = \frac{k\omega_n s}{s^2 + k\omega_n s + \omega_n^2} \qquad (2)$$

$$H_q(s) = \frac{qv'}{v}(s) = \frac{k\omega_n^2}{s^2 + k\omega_n s + \omega_n^2} \qquad (3)$$

Where ω_n represent the resonant frequency, usually $2\pi f$ rad, and k is the damping coefficient. $H_d(s)$ is the TF of the band-pass filter and $H_q(s)$ is the TF of the low-pass filter with 90 degree phase shift with respect to v' at resonant frequency ω_n. The Bode plot of the closed-loop transfer function is shown in Fig.5. Fig. 6 shows the performance of the SOGI SRF-PLL under sinusoidal and non-sinusoidal conditions. Though the small frequency variation is observed under non-sinusoidal condition as shown in Fig 6, its performance is better if compared with that of APF SRF-PLL shown in Fig. 2.

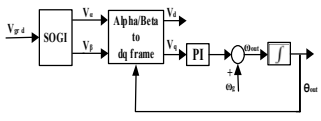


Figure 4 Schematic diagram of SOGI SRF

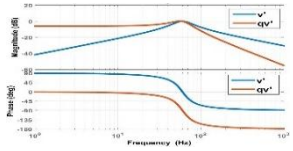


Figure 5 Bode plot response of $H_d(s)$ and

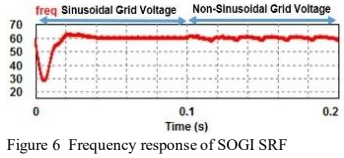


Figure 6 Frequency response of SOGI SRF

4. Purposed SOGI LPF SRF-PLL Under Sinusoidal and Non-Sinusoidal Grid Voltage Conditions

The structure of purposed SOGI LPF SRF-PLL is shown in Fig 7. The virtual signal generation technique is the same as discussed in the section 3. But in the proposed PLL structure the low pass filter is added to filter out the noise and harmonic from two phase signal v_d and v_q. The low pass filter after the park transformation is equivalent to the bandpass filter before the park transformation. As well-known, design and realization of bandpass filter require second-order or higher processing. On the other hand, low-pass filter can be designed and realized from first order. The proposed system employs the following first-order low-pass filter for simplicity as shown in Eq. (4)

$$G_l(s) = \frac{\omega_c}{s + \omega_c} \qquad (4)$$

Where ω_c is a design parameter specifying a cut-off frequency of the filter. In Fig.8 the estimated frequency has very small oscillation with respect to that with the previous techniques during 0.1s-0.2s under the non-Sinusoidal grid condition. The proposed PLL has fast dynamic under non-sinusoidal grid voltage condition and its transient response is fast enough to track the grid voltage within two cycles as shown in Fig.9.

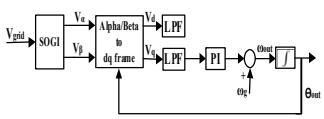


Figure 7 Schematic diagram of SOGI LPF

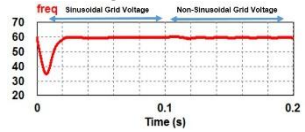
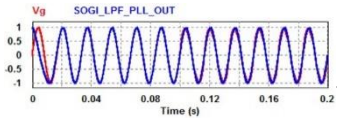


Figure8 Frequency response of SOGI LPF PLL



voltage

5. Simulation and Experimental Results

In this section, three PLL algorithms are evaluated with both simulation and experimental results under the sinusoidal and non-sinusoidal grid voltage conditions. The simulation model was implemented in PSIM and an experiments were performed with a digital signal processor TMS320F28335 by implementing the algorithms. The on-chip 12bit ADC module captures the grid voltage as an input voltage signal. The sample frequency is 10 KHz, and each PLL algorithm was executed at every interrupt service routine. The simulation and experimental results are shown in Fig. 10 and Fig.11, respectively. Each simulation waveform is shown from the top to the bottom of the figure including input grid voltage (v_g) and PLL output, virtual signal v_α and v_β, estimated frequency (freq) and phase error (Θ-Θ_{out}), respectively. Table 1 summarize the performance comparison of three PLL algorithm.

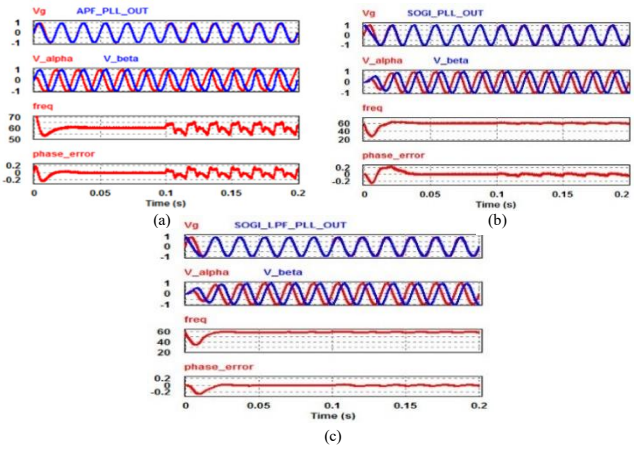


Figure 10 Simulation results: (a) APF SRF PLL, (b) SOGI SRF PLL, (c) SOGI SRF LPF PLL

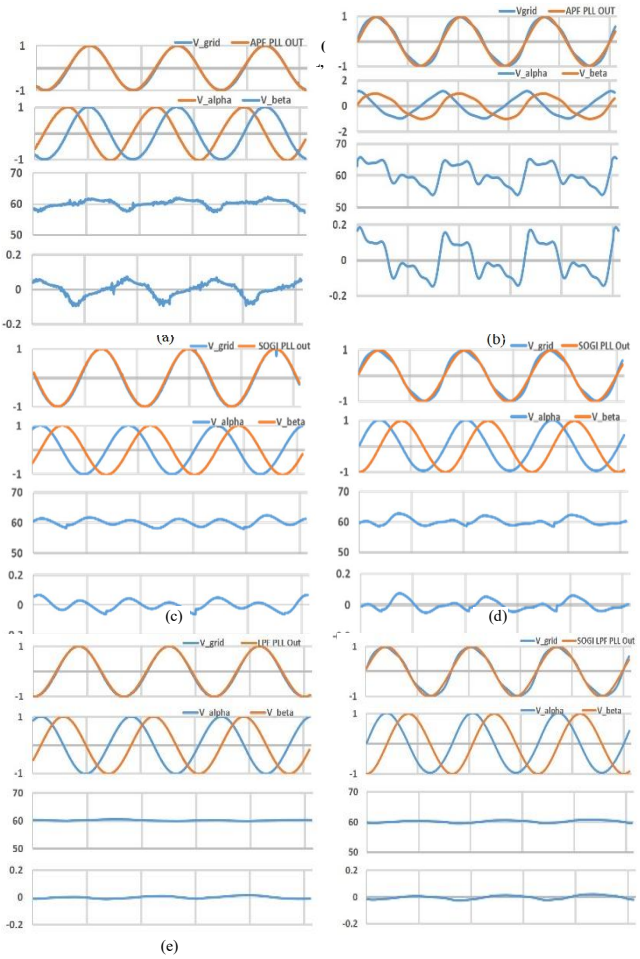


TABLE 1 Results summary for the three SRF Algorithms under non-sinusoidal grid voltage.

Figure 11 (a) APF SRF PLL under sinusoidal grid voltage, (b) APF SRF PLL under non sinusoidal grid voltage, (c) SOGI SRF PLL under sinusoidal grid voltage, (d) SOGI SRF PLL under non sinusoidal grid voltage, (e) SOGI LPF SRF PLL under sinusoidal grid voltage, (f) SOGI LPF SRF PLL under non-sinusoidal grid voltage.

TECH-NIQUES	FREQUENCY VARIATION (Hz)	STEADY STATE TIME (s)	Peak to Peak Phase Error (deg)	CONDITION
APF SRF PLL	9 6 (experimental) 9 1 (simulation)	22ms	0 35(experimental) 0 30 (simulation)	**i)** K_p = 222 1, K_i = 25181 **ii)** 2nd , 3rd, 5th grid harmonic
SOGI SRF PLL	4 1 (experimental) 3 8 (simulation)	30ms	0 15(experimental) 0 13 (simulation)	**i)** K_p = 222 1, K_i = 25181 **ii)** 2nd , 3rd, 5th grid harmonic
SOGI SRF LPF PLL	0 9 (experimental) 0 8 (simulation)	22ms	0 11(experimental) 0 09 (simulation)	**i)** K_p = 164, K_i = 52 **ii)** LPF design at 35 Hz **iii)** 2nd , 3rd, 5th grid harmonic

6. Conclusion

In this paper, a novel method to improve the performance of the PLL for single phase inverter has been proposed and its effectiveness has been verified through experiments. Three kinds of different PLL techniques are discussed by comparing the results under the sinusoidal and non-sinusoidal grid voltage conditions by using both simulation and by experiments. It has been observed that the proposed technique superior than other techniques in terms of frequency variation, fast tracking performances and small phase error.

References

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[2] L.N. Arrauda, S.M. Silva, B.J.C. Filho, PLL structures for utility connected system, Industry Applications Conference IAS, 2001, Vol. 4, pp. 2655-2660.