# 단일 전류 센서를 이용하는 새로운 브리지 없는 인터리빙 방식의 역률 보상 회로

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# A Novel Bridgeless Interleaved Power Factor Correction Circuit with Single Current Sensor

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## ABSTRACT

In this paper, a novel bridgeless interleaved power factor correction circuit with single current sensor is proposed. The proposed control strategy requires only one current sensor for the interleaved bridgeless PFC. By sampling the output current, all the boost inductor currents can be calculated and used to control the input current according to the input voltage. The reduced number of current sensors and associated feedback circuits helps reduce the cost of system. The problem caused by the unequal current gain between current sensors inherently does not exist in the proposed topology. Thus, current sharing between converters can be achieved more accurately and the high frequency distortion is decreased. In addition, the proposed technique can be applied to the other kinds of interleaved PFC topologies. Performance of the proposed control strategy is verified by the experimental results with 6.6kW bridgeless interleaved PFC circuit.

*Index Terms* – bridgeless interleaved PFC, single current sensor, digital control

## 1. Introduction

The bridgeless PFC converters have got much attention in recent years due to its superior performance in terms of efficiency compared to the conventional boost PFC converter. By utilizing the body diode of boost MOSFETs the input bridge diode can be removed and the significant amount of loss associated with it can be eliminated. In high power application, bridgeless interleaved PFC (BIPFC) saves 37% of total losses compared to conventional boost counterpart[1]. However, the high efficiency can only be achieved at the cost of high EMI noise and complex feedback circuitry.

In the conventional linear average current control scheme of boost PFC converter, the input voltage, input currents, and output voltage are measured to help the controllers shape the input current and regulate the output voltage. In BIPFC, four current transformers are typically used to indirectly sense four inductor currents by the MOSFET currents[1]. The multiple current sensor technique will increase the cost, volume, and high frequency distortion caused by unequal gain between current sensors. Other authors developed the sensorless control algorithm[2]. However, since the estimation of inductor current highly depends on the parameters of circuit, without using the current sensor, it may vary widely during the line cycle. Consequently, the waveforms are highly distorted.

In this paper, a novel BIPFC with single current sensor is proposed. By sampling the output current, the average value of the inductor currents can be calculated. Based on the calculated currents, the conventional digital control scheme with current sharing strategy can be applied effectively. A 6.6 kW PFC for level 2 on-board charger is developed to prove the validity of the proposed method.

## 2. Bridgeless Interleaved PFC with single current sensor

The BIPFC topology is shown in Fig. 1. Since the operation of this topology has already been mentioned in [1], it is focused to explain the proposed current sampling strategy of the input current. In the positive half of line cycle, the $S_1$ and $S_3$ work as active boost switches, meanwhile $S_2$ and $S_4$ work as synchronous rectifiers. During the positive half cycle, the current of inductor $L_1$ and $L_3$ should be sensed and regulated to follow the input voltage. The PWM scheme and key waveforms are shown in Fig 2. Regardless of the duty value, in the interval ($t_0$~$t_1$), the inductor $L_3$ transfers the power to the output through diode $D_3$. Thus, the input current $I_{L3}$ can be calculated by using the output current during this interval. Similarly, in the interval ($t_2$~$t_3$), the output current will be equal to the inductor $I_{L1}$. If the sampling moment is selected at the center of these intervals, the sensed current values will both represent the average value of input inductor currents exactly and be immune from switching noise. Due to the symmetrical operation of the BIPFC, the inductor $I_{L2}$ and $I_{L4}$ will be measured through the output current during the negative half of line cycle.

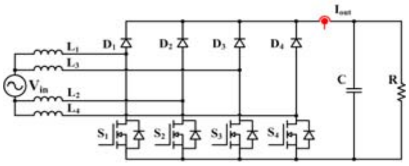


Fig. 1 Proposed Bridgeless Interleaved PFC topology with single current sensor

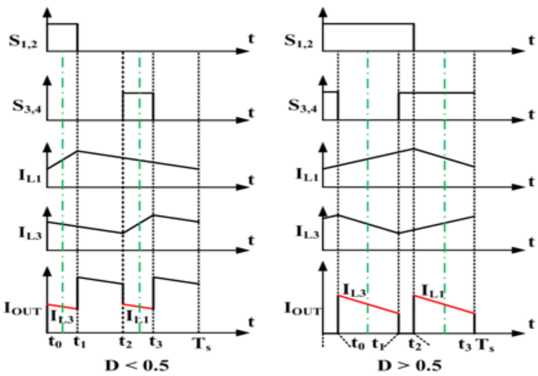


Fig. 2 Key waveforms in the BIPFC with the duty D < 0.5 and duty D > 0.5

In order to guarantee the above sampling operation, the PFC has to be designed to operate in CCM mode. In this research, a 6.6kW CCM mode BIPFC is developed. The boost inductors and output capacitor are designed with 20% current ripple and 5% of output voltage ripple based on (1) and (2) respectively. The parameters of 6.6kW BIPFC are shown in Table 1.

Table 1 Specification of proposed 6.6 kW BIPFC.

| | | |
|---|---|---|
| Input voltage | $V_{in}$ | 220 V |
| Input frequency | $f_{line}$ | 60 Hz |
| Output voltage | $V_{out}$ | 400 V |
| Rated power | $P_{out}$ | 6.6kW |
| Switching frequency | $f_s$ | 70 kHz |
| Output capacitor | $C_{out}$ | 3400 µF |
| Boost inductor | $L_{boost}$ | 120 µH |

$$L_{boost} = \frac{V_{out} \times \sqrt{2} \times D_{LL\min}}{\Delta I_L \times f_s} \quad (1)$$

$$C_{out} = \frac{2 \times P_{out}}{\eta} \frac{1}{V_{out} \times 2\pi \times 2 f_{line} \times \Delta V_{ripple}} \quad (2)$$

## 3. Digital control and current sharing strategy

The proposed digital control of bridgeless interleaved PFC is shown in Fig. 3. One outer loop is used to regulate the output voltage of the converter. The output of voltage controller with a multiplier will generate the current reference according to the input voltage for two inner current loops. These current controllers will regulate the input current according to the current reference. This control scheme guarantees the current sharing between two interleaved converters.

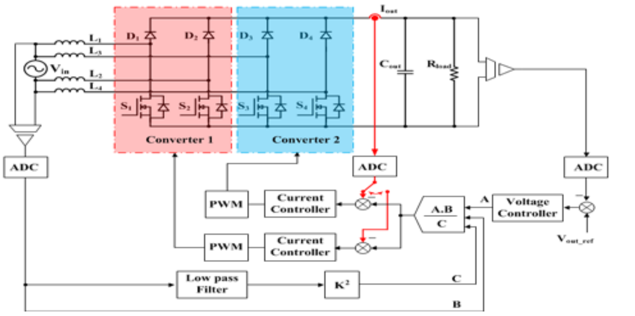


Fig. 3 Control scheme with single current sensor

The implementation method of the proposed digital control scheme with a common micro-processor based on interrupts is shown in Fig. 4. Two PWM outputs with $180^0$ phase shift are used to drive two interleaved converters. In order to fix the sampling moment of the ADC, the symmetrical PWM scheme is adopted. When the PWM counter reaches the maximum value, the module will generate the signal to start data conversion of ADC. After a conversion time delay $T_{ADC}$, the ADC result is available and the current controllers are executed in the ISR. The voltage loop can be operated in the main loop since its sampling frequency is lower. The delay time of proposed method $T_{delay}$ is equal to one cycle of PWM $T_s$. Hence, in the s-domain design, the delay time effect is modeled as a delay unit expressed by (3)

$$H_{delay}(s) = e^{-sT_s} \quad (3)$$

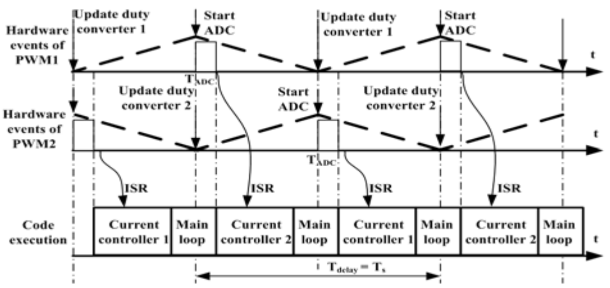


Fig. 4 Implementation of proposed digital controller in a micro-processor based on interrupt service routine

In this research, the controller is designed in the s-domain with the parameters in Table 1 including the delay in (3). The type 2 controller is used and the bandwidth of the current loop is chosen at one tenth of the switching frequency. In order to avoid the input current distortion, the bandwidth of voltage loop is chosen at one fifth of line frequency and the type 2 controller is used.

## 4. Experimental results

A 6.6kW bridgeless interleaved PFC with specification in Table 1 is designed. The digital controller is implemented using a DSP TMS320F28335. The output current is sensed by using LEM LA 100P current sensor. The key experimental waveforms are shown in Fig.4 at full load. The input current has sinusoidal waveform following the input voltage with the 4.12 % THD and 0.998 power factor. The output voltage is regulated at 400V with less than 5% 120Hz ripple.

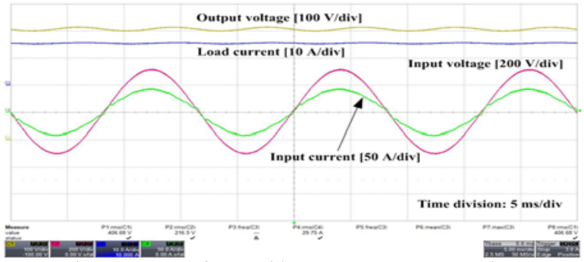


Fig. 5 Key waveforms with $V_{in}$ = 220V, Pout = 6.6 kW

The efficiency profiles obtained with the variations in input voltage are shown in Fig. 6. The high efficiency is maintained over the wide range and the maximum value is 98.8% at $V_{in}$ = 265V. The input power factor curves are shown in Fig. 7 and the power factor can be achieved greater than 0.99 from half load to full load at 220V AC input voltage.

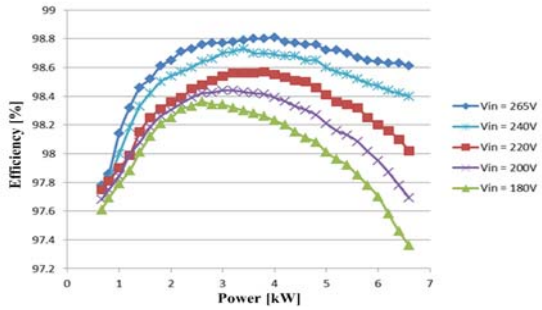


Fig. 6 Efficiency profile of proposed BLPFC

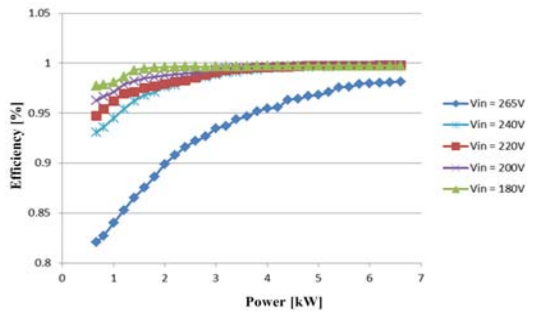


Fig. 7 Power factor profile of the proposed BIPFC

## 5. Conclusion

In this paper, a novel bridgeless interleaved PFC with single current sensor is presented. The sampling technique and digital control scheme with a single current sensor are proposed. With the proposed technique, the conventional linear average current control scheme can be successfully adopted with single current sensor. Since the proposed converter is compact, simple, and highly efficient, it is suitable for single phase PFC for level 2 on-board battery charger. The feasibility of the proposed method has been verified by implementing a 6.6kW PFC converter.

## References


[1] F. Musavi, et al., "A High-Performance Single-Phase Bridgeless Interleaved PFC Converter for Plug-in Hybrid Electric Vehicle Battery Chargers," in IEEE Transactions on Industry Applications, vol. 47, no. 4, pp. 1833-1843, 2011.

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