SRP 기반 FHD HEVC Decoder

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SRP Based Programmable FHD HEVC Decoder

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요 약

A programmable video decoding system with multi-core DSP and co-processors is presented. This system is adopted by Digital TV SoC (System on Chip) and is used for FHD HEVC (High Efficiency Video Coding) decoder. Using the DSP based programmable solution, we can reduce commercialization period by one year because we can parallelize algorithm development, software optimization and hardware design. In addition to the HEVC decoding, the proposed system can be used for other application such as other video decoding standard for multi-format decoder or video quality enhancement.

1. INTRODUCTION

Recently embedded systems should support a wide range of video standards. New video standards (VP8, HEVC[1]) as well as existing ones should be supported at multimedia devices. In case of full hardware approach, It is necessary to make a new SoC to support a new video standard. If the SoC has processor based video solution then the SoC does not need to change a new one. Another merit of processor based approach is that commercialization period can be saved dramatically because the hardware can be developed based on existing processor and the software can be optimized in parallel with the hardware development.

In spite of the advantages of processor based approach, it has weakness compared to full hardware approach. Y. Kikuchi et al [2] used a hybrid approach to trade-off between flexibility and performance. They used full hardware to support H.264 [3] with 1080p resolution which has the most complexity among existing video standards at that time. Flexibility is considered by adopting multi-core processor to support other video standards. As the most complex video standard is realized by full hardware this method has limitations for future extensions. For example they have to fabricate a new chip to support HEVC because the HEVC have more complexity than that of H.264. For this reason we develop a video decoding system with full programmable feature.

In this paper we propose a video decoding system composed of two SRPs (Samsung Reconfigurable Processor) and two special purpose co-processors. We can get high performance and flexibility using the SRP because it has massive parallel computing architecture and programmable feature. Bitstream decoding and SDRAM accessing performance are enhanced by BsPU (Bitstream Processing Unit) and MemPU (Memory Processing Unit) respectably.

Because the HEVC standard was not fixed when we started developing the SRP based system, we developed the software and the system architecture development in parallel following the HEVC standard progressive. By using this parallel development method, we could reduce the commercialization period by one year.

The remainder of this paper organized as follows. Section II gives an overview of the SRP. In section III, problems of processor based system are described in terms of video decoding application. The proposed video decoding system is presented in section IV. The experimental results and conclusion is followed in section V and section VI respectively.

2. OVERVIEW OF RECONFIGURABLE PROCESSOR

The basic SRP architecture is a coarse-grained array and reconfigurable architecture [4]. The SRP is consisted of a coarse-grained array of functional units (FU), global and local register files, instruction cache, internal memory, configuration memory, and several bus connections for off-

chip data transfer. The FUs are arranged on a NxM grid. In this paper 4x4 grid is used.

The SRP has two operation modes: Very Long Instruction Word (VLIW) and Coarse-Grained Array (CGA). In VLIW mode, the SRP behaves like a general purpose n-issue VLIW processor. The 2-issue was used for video system in this paper, which implies 2 FU out of 16 FU was used in VLIW mode. VLIW mode is used for sequentially or infrequently executed code. In CGA mode, the SRP operates in data flow mode. In other words, there is no control flow. All entities are programmed via bits in so-called configuration memories. CGA mode can exploit loop level parallelism with all FUs and has good performance at repetitive arithmetic operations.

3. PROBLEM DEFINITION

We identified three disadvantages of SRP for video applications. The first is that the SRP is very inefficient for VLD (Variable Length Decoding), which has very strong dependencies between operations. The SRP can execute 16 instructions in one cycle but the average instructions per cycle of VLD are about 1.5.

The second is huge memory bandwidth which results in waste of time for data transfer. In case of video decoding application major memory bandwidth is consumed by fetching the reference frame data for motion compensation.

The third is low CGA efficiency due to heavy control operations of video decoding application. The control operations cannot be mapped in CGA but in can be mapped in VLIW. In VLIW mode only 2 FUs are in operation out of 16 FUs, which result in very low resource utilization.

To overcome these disadvantages, we introduce BsPU and MemPU to accelerate bitstream decoding and memory access respectably. To increase resource utilization a new parallelization architecture is developed.

4. PROPOSED DECODING SYSTEM

In this section, the proposed decoding system is described shown in Fig. 1. The proposed decoding system is composed of a BsPU, a MemPU and two SRP.

The bitstream decoding function is accelerated by using special instructions of BsPU. The SDRAM bandwidth is reduced by using MemPU. Performance enhancement is realized through dual thread parallel execution architecture.

A. Bitstream Processing Unit (BsPU)

The processing flow of VLD is composed of bit acquisition, table mapping, and bit position update. These operations take 24 cycles using basic instructions of SRP. We accelerated the bit acquisition and position update by using bitstream manipulation instructions. These instructions share a common hardware to buffer input bitstream from SDRAM, bit manipulation logic, and detection of three byte emulation prevention code.

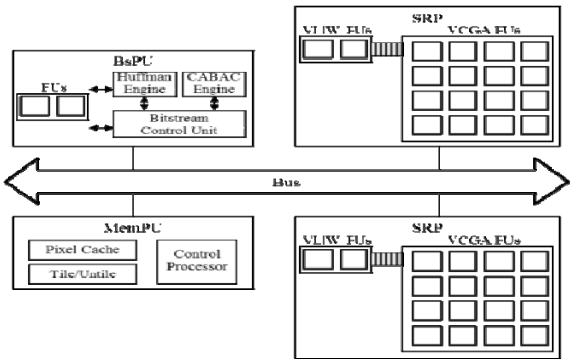

Fig. 1. System block diagram of video decoding system

B. Memory Processing Unit (MemPU)

The function of the memory processing co-processor is transferring data between external memory and internal memory of SRP with minimum bandwidth. By adopting tile based SDRAM access we can reduce wasted cycle by SDRAM latency. The number of SDRAM access is reduced by using a pixel cache which has 3-D feature (2-D block position and time). The detailed of the tiled memory access and the pixel cache are described in our previous paper [4]. Additionally we adopted the multiple outstanding feature of AMBA3 AXI. The co-processor of memory processing give multiple read commands to SDRAM controller and the SDRAM controller schedule the SDRAM and transfer data to memory processing co-processor.

C. Dual Thread Parallel Execution

The characteristic of video decoding application is that it has many control operations. The major control operations are motion vector decoding, mode decision including intra and inter mode. As shown in Fig. 2 (a) half of total cycle is consumed in VLIW mode. In VLIW mode only 2 FUs are operational, which results in computing resources in 14 FUs are wasted in VLIW mode.

The resource utilization can be dramatically improved by parallelize the VLIW and CGA mode as shown in Fig. 3 (b). The control operations are performed in one block proceeding to the computational operations to parallelize the two operational modes. Parameters for the computational operations are drawn by the control operations and transferred via a FIFO between the VLIW and CGA.

5. Experimental Results

We implemented our video decoding system on a DTV SoC chip and evaluated the performance. The SoC was fabricated by using Samsung 45nm process and operation frequency of the proposed video decoding system is 400MHz.

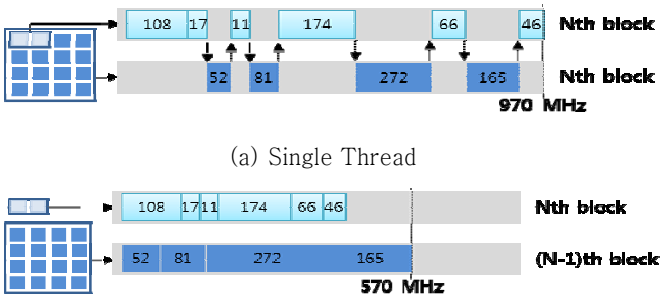

Fig. 2. Resource utilization enhancement using dual thread parallel execution

We implemented HEVC main profile software in the proposed video decoding system with FHD resolution (1920x1080) and frame rate of 30 frames per second. The HEVC main profile software is fully verified by using ALLEGRO bitstream. The required operation frequency for real-time decoding of FHD 30 frames per second HEVC stream with 8M bit per second is about 370MHz.

TABLE I
REQUIRED CLOCK CYCLES FOR REAL-TIME DECODE OF HEVC

Resolution	Bitrate	Required Clock
1920x1080	8Mbps	370MHz

6. CONCLUSION

This paper proposes a SRP based video decoding system, which can decode FHD HEVC stream in real time. The system is composed of a BsPU, a MemPU, and two SRPs. Bitstream decoding is accelerated by the BsPU. Memory bandwidth is reduced by MemPU. Other functions are driven by the two SRPs.

We also explored new dual thread parallel execution architecture. By adopting the architecture we could enhance the performance about 41% compared to single thread architecture. The video decoding system is embedded in DTV SoC and commercialized for FHD HEVC decoding application. Using the SRP based programmable solution, we can reduce commercialization period by one year because the hardware can be developed based on existing processor and the software can be optimized in parallel with the hardware development.

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