불평형 부하에서 강인한 3상4족 전압형 인버터를 위한 하이브리드 제어기의

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Design of the Robust Hybrid Controller for Three-Phase Four-Leg Voltage Source Inverter under the Unbalance Load

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ABSTRACT

The three-phase four-leg voltage source inverter (VSI) topology can be an interesting option for the three phase-four wire system. With an additional leg, this topology can achieve superior performance with unbalanced and/or nonlinear load. This paper proposes a new hybrid controller which combines PI controller and resonant controller in synchronous frame for three phase four leg inverter. The hybrid controller is simple in structure and easy to implement. The performance of proposed controller is verified by the experiments and compared with that of the conventional PI controller.

Index Terms – Three-phase four-leg, 3D SVM, Unbalanced load condition, Resonant controller, Hybrid controller.

1. Introduction

Recently, the three phase four leg inverter has been an interesting option to provide the neutral wire for the small distributed system. In comparison with other topologies, the three phase four leg topology has salient advantages such as compact size, fast response, small DC link capacitance, and higher modulation index. However, when working in fault mode or in the presence of single load, the unbalanced currents will flow through the power supply having finite output impedance and it causes an output voltage distortion. One solution for solving the problem is the separate rotating frame method ^[2]. However, the method requires a quite complex structure and time-consuming algorithm. In the following sections, the details about the control strategy of the hybrid controller to guarantee the balanced output voltage under the unbalanced load condition are presented.

2. Modeling of three-phase four-leg inverter with unbalanced load in the synchronous frame

2.1 Modeling of three phase four leg inverter in the synchronous frame

Fig. 1 shows the three phase four leg inverter topology. Assuming that all the switches are ideal, the output voltage and DC link current can be expressed as (1) and (2), respectively.

$$\begin{bmatrix} V_{af} & V_{bf} & V_{cf} \end{bmatrix}^{T} = \begin{bmatrix} d_{af} & d_{bf} & d_{cf} \end{bmatrix}^{T} \cdot V_{DC}$$
(1)
$$i_{p} = \begin{bmatrix} d_{af} & d_{bf} & d_{cf} \end{bmatrix} \begin{bmatrix} i_{a} & i_{b} & i_{c} \end{bmatrix}^{T}$$
(2)

where $[d_{af} \ d_{bf} \ d_{cf}]$ is the phase leg ratio vector; $[V_{af} \ V_{bf} \ V_{cf}]$ is output voltage vector; $[i_a \ i_b \ i_c]$ is output current vector; V_{DC} and i_p are DC-link voltage and current, respectively.

By applying Kirchhoff's laws and Park transformation to the system shown in Fig. 1, the model for d-channel in the synchronous coordinates is given by (3).

$$\frac{\mathrm{d}}{\mathrm{dt}} \begin{bmatrix} \mathrm{V}_{\mathrm{d}} \\ \mathrm{I}_{\mathrm{d}} \end{bmatrix} = \begin{bmatrix} 0 & 1/C \\ -1/L & 0 \end{bmatrix} \begin{bmatrix} \mathrm{V}_{\mathrm{d}} \\ \mathrm{I}_{\mathrm{d}} \end{bmatrix} + \begin{bmatrix} 0 \\ \mathrm{V}_{\mathrm{DC}}/L \end{bmatrix} \mathrm{d}_{\mathrm{d}} + \begin{bmatrix} -1/C \\ 0 \end{bmatrix} \mathrm{I}_{\mathrm{Ld}}$$
(3)

Where, V_d is the output voltage, I_d is the output current, I_{Ld} is the load current, and d_d is the phase leg ratio on d-channel.

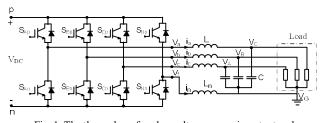


Fig. 1. The three-phase four-leg voltage source inverter topology From (3), the transfer function of the control-to-output voltage on d-channel can be obtained as (4). The q-channel transfer function is the same with d-channel.

$$G_{d}(s) = \frac{V_{d}}{d_{d}} = \frac{V_{DC}}{LCs^{2} + \left(\frac{L}{R_{Load}}\right)s + 1}$$
(4)

Similarly, the transfer function of the control-to-output voltage on o-channel is given by (5).

$$G_{o}(s) = \frac{V_{o}}{d_{o}} = \frac{V_{DC}}{(L+3L_{n})Cs^{2} + \left(\frac{L+3L_{n}}{R_{Load}}\right)s+1}$$
(5)

From (4) and (5), under full load, the system is the conventional second order system with under damped characteristic; however, under light load, the resonant peak becomes very high, and the phase drops to -180 degree steeply. In order to design the compensator for this type of transfer function, the PI controller can be employed to provide zero steady state error. However, the bandwidth of system may not be high enough to satisfy the stability margin at light load contint.

2.2 Modeling of unbalanced load current in the synchronous frame

The unbalanced load current can be decomposed into symmetric components with positive sequence, negative sequence and zero sequence currents as (6).

$$\begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} = \begin{bmatrix} I_{Lap} \\ I_{Lbp} \\ I_{Lcp} \end{bmatrix} + \begin{bmatrix} I_{Lan} \\ I_{Lbn} \\ I_{Lcn} \end{bmatrix} + \begin{bmatrix} I_{Lao} \\ I_{Lbo} \\ I_{Lco} \end{bmatrix}$$
(6)

Applying Park's transformation to the components, the symmetric components of load current in synchronous frame can be obtained as (7), (8) and (9).

 $\begin{bmatrix} I_{Ldp} & I_{Lqp} & I_{Lop} \end{bmatrix}^{T} = \sqrt{2} I_{Lp} [\cos\varphi_{p} - \sin\varphi_{p} \quad 0]^{T}$ (7) $\begin{bmatrix} I_{Ldn} & I_{Lqn} & I_{Lon} \end{bmatrix}^{T}$

$$= \sqrt{2}I_{\text{Ln}}[\cos(2\omega t + \varphi_n) - \sin(2\omega t + \varphi_n) \quad 0]^{\text{T}}$$
(8)

 $[I_{Ldo} \quad I_{Lqo} \quad I_{Loo}]^{T} = \sqrt{2} I_{Lo} [0 \quad 0 \quad \cos(\omega t + \varphi_{0})]^{T}$ (9) where,

 $\begin{bmatrix} I_{Ldp} & I_{Lop} \end{bmatrix}^T, \begin{bmatrix} I_{Ldn} & I_{Lqn} & I_{Lon} \end{bmatrix}^T, \begin{bmatrix} I_{Ldo} & I_{Lqo} & I_{Loo} \end{bmatrix}^T \\ \text{are positive, negative, and zero sequence components of load current in the synchronous frame, respectively. <math>\phi_p, \phi_n, \phi_o$ are leading angles of symmetric components. ω is the angular velocity of the positive sequence component.

From (7), (8) and (9), it can be seen that under unbalanced load condition, the negative sequence and zero sequence currents appear as harmonics with frequency of 2ω on the d/q channels, and frequency of ω on the o channel, respectively. However, the

conventional PI controller cannot eliminate these noises due to its low bandwidth. Thus, these currents cause the voltage drop on the output impedance of power supply and the phase voltage at the output terminal is unbalanced consequently.

3. Proposed hybrid controller for three phase four leg inverter under unbalanced load

Under the unbalanced load condition, it is possible to provide balanced voltages if the noises caused by negative and zero sequence components in synchronous frame are eliminated. In this research, a hybrid controller which combines PI and resonant controller (PI+R) is proposed. The PI controller with infinity gain at DC frequency can guarantee the zero steady state error of positive sequence voltage. In order to eliminate unbalanced voltage caused by negative and zero sequence voltages, the resonant controllers are designed to have peak gain at 2ω frequency on d/q channels and at ω frequency on o channel, respectively.

The transfer function of hybrid controller is given by $(10)^{[1]}$.

$$C(s) = K_p + \frac{K_I}{s} + \frac{2K_R s}{s^2 + \omega_0^2}$$
(10)

The structure of hybrid controller (PI+R) is shown in Fig. 2

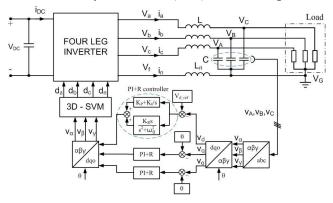


Fig. 2. Block diagram of the hybrid controller for three phase four leg inverter

The Bode plot of d-channel is shown in Fig. 3 with the design parameters are as followings: output power $P_{out} = 3 \text{ kW}$, DC-link voltage $V_{DC} = 400$ V, output line-line voltage $V_{out} = 220$ V, switching frequency $f_{PWM} = 10$ kHz, and output frequency $f_{out} = 60$ Hz. The parameters of the output filter are L = 2.5 mH, C = 10 μ F, and L_n = 1.2 mH on the neutral wire. The controller on d/q channel are designed with following parameters: $K_i = 0.21$, $K_p = 3.78e$ -5, $K_r = 0.05$, $\omega_0 = 754$ (rad/s). The o channel controller has $K_i = 0.16$, $K_p = 4.59e$ -5, $K_r = 0.1$ and $\omega_0 = 377$ (rad/s).

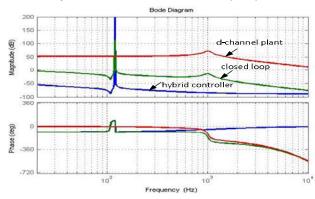
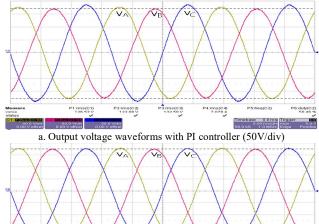


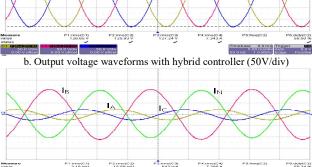
Fig. 3. Bode plot of the d-channel plant, the hybrid controller and the closed-loop system

4. Experiment results

A 3kW prototype was built to verify the proposed method. The 3D SVM algorithm and controllers are implemented in a DSP TMS320F28335. The experimental results are shown in Fig.4 and Table 1.

As shown in Fig. 4, under heavy unbalanced load conditions, the proposed controller can guarantee the balance output phase voltage while the PI controller shows poor performance. For the comparison of the two methods, the output voltage in each case was measured by Fluke 435 power quality analyzer as shown in Table 1.





c. Output load current waveforms with hybrid controller (ch1: 2A/div, ch2: 5A/div, ch3: 2A/div, ch4: 5A/div) Fig. 4. Performance comparison between two methods under unbalanced load (10% load on phase A and C; full load on phase B)

Table 1. Quality of the output voltage in two methods (Case 1: phase A 10% load, phase B, C full load; Case 2: phase A,C 10% load, phase B full load)

Condition	Controller	Negative sequence component (%)	Zero sequence component (%)
Case 1	PI	2.2	5.8
	Hybrid	0.1	0.6
Case 2	PI	2.2	5.9
	Hybrid	0.3	0.5

5. Conclusion

In this paper, a hybrid controller is proposed for the three phase four leg inverter under unbalanced load. The hybrid controller is simple in structure and easy to implement. It is proved that the proposed controller can provide the balanced output voltages under the highly unbalanced load condition.

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