A novel PLL control method for robust three-phase thyristor converter under sag and notch conditions

Changhee Lee, Hyoyol Yoo

Department of Research and Development, Dawonsys
227, Gyeonggigwagidae-ro, Siheung-si, Gyeonggi-do, Korea
Email: chlee@dawonsys.com

Abstract

The paper presents a novel phase locked loop(PLL) control method for robust three-phase thyristor dual converters under sag, notch, and phase loss conditions. This method is applied to three line to line voltages of grid to derive three phase angle errors from three separated single-phase PLLs. They can substitute for abnormal phase to guarantee the synchronization in the various grid fault conditions. The performance of novel PLL with moving average method is verified through simulations.

Keywords: extended single-phase PLL, grid voltage, line notching, phase angle, voltage sag.

1. Introduction

Synchronization plays an important role in control of three-phase AC/DC converter or thyristor dual converter connected to grid. Fig. 1 shows the configuration of thyristor dual converter. The phase angle of grid voltage is the referred value for determining the firing angle of thyristor converters. Therefore, the performance of converters will be significantly reduced if there is an error in firing angle [1]. Three-phase PLLs have been widely used for three-phase system due to the simple, stable and robust to estimate phase angle under the ideal condition. However under grid voltage sag and/or line notching, the estimated phase angle becomes distorted [2][3]. In order to overcome these drawbacks, the paper proposed an extended single-phase PLL which can reconstruct the reference voltage from the phase angle of normal line to line voltages in the presence of sag and/or line notching in the grid.

2. Extended single-phase PLL

The common approach of single-phase PLL is the generation of a virtual signal with the phase lag of 90° from the original signal. These signals considered as the *d*, *q* components in the stationary frame are transformed to synchronous reference frame using the Park transformation. The estimated angle θ_{est} is obtained by integrating frequency at the output of the proportional-integral (PI) regulator that use the synchronous *d*-axis voltage as the phase angle error.

In the proposed method, these errors are derived through three line to line voltages V_{ab}, V_{bc} and V_{ca}. The line to line voltage V_{ab} is defined as a base voltage. To identify other phase angle errors with base phase, the *d*, *q* components of both V_{bc} and V_{ca} at the stationary frame are shifted by angle of 120° and -120°, respectively. The phase angle errors of line to line voltages which are the *d*-axis voltages can be approximated in *pu* as following [3]

$$\begin{aligned} e_{d1} &\approx \theta_{err1} = \theta_{est} - \theta_{ab} \\ e_{d2} &\approx \theta_{err2} = \theta_{est} - \theta_{bc} + 120^\circ \\ e_{d3} &\approx \theta_{err3} = \theta_{est} - \theta_{ca} - 120 \end{aligned} \quad (1)$$

where e_{d1}, e_{d2} and e_{d3} are the *d*-axis line to line voltages in *pu*; θ_{ab}, θ_{bc} and θ_{ca} are the phase angle of line to line voltages; θ_{est} is the estimated phase angle.

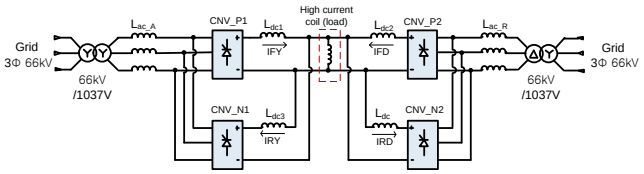

Fig. 1. Configuration of a thyristor dual converter.

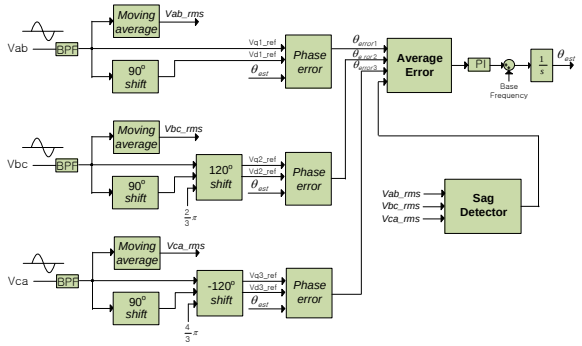

Fig. 2. Extended single-phase

Besides, a phase shift of 90° is simply attained by using an first-order all-pass filter as following [3]

$$Y(s) = \frac{-\mathrm{bs}+1}{\mathrm{bs}+1} X(s) \quad (2)$$

where $b = 1/2\pi f$, f is the grid frequency.

3. Voltage sag detection and average error

Voltage sag is detected when the RMS voltage drop below the specific threshold which is defined as *0.85* [pu] in this paper. The RMS voltage of three-phase line to line voltages is calculated from sample data using a one-cycle window by [4]

$$V_{rms} = \sqrt{\frac{1}{\mathrm{N}} \sum_{j=0}^{N-1} V_j^2} \quad (3)$$

where *N* is the number of sample points per cycle of fundamental, V_j is the j^{th} sample of the recorded voltage waveform. Based on the moving average RMS technique, the digital controller can calculate and update the RMS values many times per line-frequency cycle. Therefore, the occurrence of sag can be a faster detection.

Three sag detection signals are the logic signals which can derive total eight modes corresponding to eight angle error values. Depends on the fault situation, the phase angle error, which is the input to PI regulator, can be obtained by the average of the angle errors of the normal phases. In case of three-phase fault where RMS voltage of all line to line voltages drop below the threshold value, the input to PI regulator is set to zero and the synchronous signal is the latest normal line to line voltage. The selection technique is also applied to eliminate the phase angle error of a sag voltage from the calculation of average error. Fault situations and corresponding average error is shown in Table 1.

TABLE 1
FAULT SITUATIONS AND CORRESPONDING AVERAGE ERROR

Mode	Line voltage sag	Average error
1	*No fault*	$(\theta_{err1}+\theta_{err2}+\theta_{err3})/3$
2	V_{ca}	$(\theta_{err1}+\theta_{err2})/2$
3	V_{bc}	$(\theta_{err1}+\theta_{err3})/2$
4	V_{ab}	$(\theta_{err2}+\theta_{err3})/2$
5	V_{bc}, V_{ca}	θ_{err1}
6	V_{ab}, V_{ca}	θ_{err2}
7	V_{ab}, V_{bc}	θ_{err3}
8	V_{ab}, V_{bc}, V_{ca}	*0*

The hysteresis band(*0.85*pu~*0.9*pu) is also applied to reduce the instability of control method at the instant of mode change.

4. Simulation Results

The extended single-phase PLL applied to thyristor dual converter under voltage sag and/or line to line notching had been verified by simulation results. The primary and secondary line to line voltages of grid transformer are *66* [kV] and *1037* [V], respectively. DC load is a *50* [mH] high current coil with the maximum current capacity at ± 50 [kA]. Fig. 3 shows the control performance of proposed technique to the voltage sag. Voltage sags of line to line voltages V_{ab}, V_{bc} and V_{ca} is introduced at the instant of *0.4*, *0.6* and *0.8* sec, respectively. RMS values are calculated and fast updated to notice the occurrence of sag. Depending on the fault situation, the mode changes from *1* to *8* which results in the different average error values. As can be seen in Fig. 3(f), (g), the average error illustrates the good tracking performance and quickly response to the change of fault mode. Fig. 3(h) shows result of the estimated angle, θ_{est}, which is achieved an accurate performance under voltage sags of line to line voltages. Consequently, the estimated waveform of three-phase voltages in Fig. 3(b)-(d) can be recovered from other normal phases. The tracking performance of extended single-phase PLL under amplitude sag and notching is shown in Fig. 4. The results also show preciously estimated line to line voltages.

5. Conclusion

The paper proposed a novel PLL with average error method for synchronization in control of three-phase thyristor dual converter. The simulation results under voltage sag and/or line notching show the feasibility of proved control technique. The reference voltage can be reconstructed from the normal phases in occurrence sag. The fault mode had been identified and the corresponding phase error had been derived. The good performance of synchronization in various type of grid fault condition leads to the improvement of stability in controlling three-phase thyristor dual converter.

References

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(a)

(b)

(c)

(d)

(e)

(f)

(g)

(h)

Fig. 3. Simulation results under voltage sag (a)Pre-program grid voltage; (b), (c), (d) estimated voltage and grid voltage of line voltages; (e) rms value of line voltages; (f) fault mode; (g) angle error; (h) estimated angle.

(a)

(b)

(c)

(d)

(e)

(f)

(g)

(h)

Fig. 4. Simulation results under voltage sag and line notching (a)Pre-program grid voltage; (b), (c), (d) estimated voltage and grid voltage of line voltages; (e) rms value of line voltages; (f) fault mode; (g) angle error; (h) estimated angle.

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