

# 3상 4레그 전압형 인버터를 위한 3차원 공간벡터변조 기법

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## 3-Dimensional SVM Technique for the Three-Phase Four-Leg Voltage Source Inverter System

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### ABSTRACT

The three-phase four-leg voltage source inverter (VSI) topology can be an interesting option for the three phase-four wire system. With an additional leg, this topology can handle the neutral current, hence the DC link capacitance can be reduced significantly. In this paper the three dimensional space vector modulation (3D SVM) in  $\alpha\beta\gamma$  coordinates for the three-phase four-leg VSI is presented. By using the 3D SVM method, the DC link voltage can be reduced by 16% compared with the split DC link capacitor topology and the output distortion can also be reduced under the unbalanced load condition.

*Index Terms* – Three-phase four-leg, voltage source inverter, 3D SVM, Unbalanced load condition, output distortion

### 1. Introduction

In a three-phase four-wire system, zero sequence components occur when the load is not balanced. In this case, the power supply system requires some means to handle it. Several solutions have been proposed to solve the problem such as three phase converter with an output zigzag or delta-star transformer, the three-phase four-wire topology with split DC link capacitor, and the three-phase four-leg topology [1-3]. Among them, the three-phase four-leg topology has salient advantages such as: compact size, fast response, ability to handle the zero sequence current and a small DC link capacitance compared with the split DC link capacitor topology [3].

As the conventional three-phase converter, the three-phase four-leg inverter can be modulated with various types of carrier based PWM or space vector modulation (SVM) method. Thanks to SVM method, the three-phase four-leg topology can achieve higher DC voltage utilization and a lower harmonic distortion under unbalanced load condition. Although the reference space vector can be synthesized either in  $\alpha\beta\gamma$  coordinates or abc coordinates [1], the former is more favorable due to the easiness in the analysis and control of the zero-sequence component. In this paper the three dimensional space vector modulation method in  $\alpha\beta\gamma$  coordinates is detailed for three-phase four-leg inverter system.

### 2. Definition of three dimensional vector

Assuming that the switches are ideal, the switch model of the three-phase four-leg inverter is obtained as shown in Fig. 1.

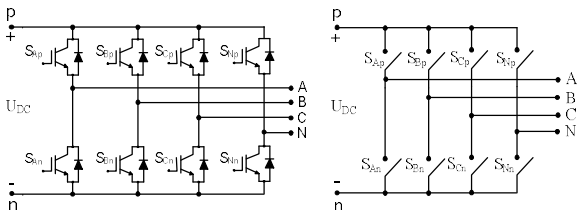


Fig. 1 The three-phase four-leg topology and switching model

There are 16 possible combinations of the switches. Each combination is represented by switching vector  $[S_A S_B S_C S_N]$  in natural coordinates, where the  $S_i$  ( $i = A, B, C, N$ ) has one of two

values at a given time: p – when the leg  $i$  connects to positive rail, and n – when the leg  $i$  connects to negative rail. Each combination has fixed output voltages as listed in the Table 1.

Table 1 Possible switch combinations and its output voltages

Voltages	Combinations							
	pppp	nnnp	pnnp	ppnp	npnp	nppp	nnpp	pnpp
$V_A$	0	$-V_{DC}$	0	0	$-V_{DC}$	$-V_{DC}$	$-V_{DC}$	0
$V_B$	0	$-V_{DC}$	$-V_{DC}$	0	0	0	$-V_{DC}$	$-V_{DC}$
$V_C$	0	$-V_{DC}$	$-V_{DC}$	$-V_{DC}$	$-V_{DC}$	0	0	0
	pppn	nnnn	pnnn	ppnn	npnn	nppn	nnpn	pnpn
$V_A$	$V_{DC}$	0	$V_{DC}$	$V_{DC}$	0	0	0	$V_{DC}$
$V_B$	$V_{DC}$	0	0	$V_{DC}$	$V_{DC}$	$V_{DC}$	0	0
$V_C$	$V_{DC}$	0	0	0	0	$V_{DC}$	$V_{DC}$	$V_{DC}$

In order to develop the vector space in  $\alpha\beta\gamma$  coordinates, the switching vectors in this frame must be established by applying the Clark transformation  $T$  to the switching vectors in the natural coordinates as shown in the Table 1. Thus, the vector space in the  $\alpha\beta\gamma$  coordinates of three-phase four-leg inverter can be obtained as shown in the Fig. 2. Due to the zero-sequence component, the vector space has a three dimensional structure. When the load is balanced, the zero-sequence component is equal to zero and the trajectory of the vector is inside the central hexagon. It is straight forward to find out that the maximum modulation index ( $M_{max}$ ) equals to 1, which is 16% higher than that of the other topology under the balanced load condition.

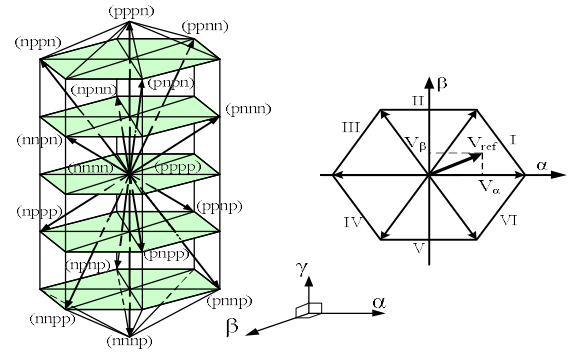


Fig. 2 The vector space of three-phase four-leg inverter in  $\alpha\beta\gamma$  coordinates

### 3. 3D SVM Scheme

Similar to the conventional 2D SVM algorithm, the 3D SVM method involves following steps: (1) selection of the switching vectors, (2) synthesis of the reference output vector, (3) sequencing of the vectors in the PWM scheme.

Firstly, in order to determine the switching vectors, the vector space is divided into six prisms. This step can be performed in a similar way as done by the conventional SVM by taking into account the  $\alpha, \beta$  components of the reference output voltage. Each prism has four tetrahedrons identified by the sign of phase voltages and each tetrahedron has three adjacent non-zero switching vectors and two zero switching vectors at the origin.

The next step is the synthesis of the reference vector based on the selected switching vectors. To achieve lowest output distortion and minimum switching loss, the nearest switching vectors should be selected. Assuming that the tetrahedron containing the reference voltage vector  $\mathbf{V}_{ref}$  has three adjacent non-zero switching vectors  $\mathbf{V}_1$ ,  $\mathbf{V}_2$  and  $\mathbf{V}_3$  as shown in the Fig.3, the vector  $\mathbf{V}_{ref}$  can be synthesized as (1).

$\mathbf{V}_{ref} = d_1\mathbf{V}_1 + d_2\mathbf{V}_2 + d_3\mathbf{V}_3$  (1)  
where  $d_1$ ,  $d_2$  and  $d_3$  are the duty ratio of each vector.

The equation (1) can be expanded as (2).

$$\begin{bmatrix} V_{ref,\alpha} \\ V_{ref,\beta} \\ V_{ref,\gamma} \end{bmatrix} = \begin{bmatrix} V_{1,\alpha} & V_{1,\beta} & V_{1,\gamma} \\ V_{2,\alpha} & V_{2,\beta} & V_{2,\gamma} \\ V_{3,\alpha} & V_{3,\beta} & V_{3,\gamma} \end{bmatrix} \begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} \quad (2)$$

where  $V_{i,\alpha}$ ,  $V_{i,\beta}$  and  $V_{i,\gamma}$  are the  $\alpha$ ,  $\beta$ ,  $\gamma$  element of the  $\mathbf{V}_i$  vector ( $i = 1, 2, 3, ref$ )

From (2), the duty ratios for non-zero switching vectors can be obtained as (3) and (4)

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \begin{bmatrix} V_{1,\alpha} & V_{1,\beta} & V_{1,\gamma} \\ V_{2,\alpha} & V_{2,\beta} & V_{2,\gamma} \\ V_{3,\alpha} & V_{3,\beta} & V_{3,\gamma} \end{bmatrix}^{-1} \begin{bmatrix} V_{ref,\alpha} \\ V_{ref,\beta} \\ V_{ref,\gamma} \end{bmatrix} \quad (3)$$

$$\mathbf{d} = \frac{1}{V_{DC}} \mathbf{M}^{-1} \mathbf{V}_{ref} \quad (4)$$

where  $\mathbf{d}$  is the duty ratio vector and  $\mathbf{d} = [d_1 \ d_2 \ d_3]^T$ ,  $\mathbf{M}$  is the matrix of elements of three non-zero switching vectors,  $\mathbf{V}_{ref}$  is the reference vector  $\mathbf{V}_{ref} = [V_{ref,\alpha} \ V_{ref,\beta} \ V_{ref,\gamma}]^T$ .

The rest of PWM period is for zero switching vectors.

$$d_z = 1 - (d_1 + d_2 + d_3) \quad (5)$$

Since when the reference vector moves to other tetrahedron, only matrix  $\mathbf{M}$  in (4) changes, 24 matrices exist with 24 tetrahedrons, respectively.

After determining the duty ratios, switching vectors are arranged in one switching period. Many switching sequences have been proposed for inverter to reduce the switching loss and the harmonics. In this research, the symmetrical sequence is used to obtain the lowest output distortion. Two zero switching vectors are used in each switching period.

#### 4. The simulation and experiment results

The simulation was performed by using Matlab Simulink tool. The simulation parameters are as followings:  $V_{DC} = 700V$ , output voltage  $V_{out} = 220 V$ , switching frequency  $f_{PWM} = 5 \text{ kHz}$ , and output frequency  $f_{out} = 50 \text{ Hz}$ . Under balanced load  $R_{load} = 5\Omega$ ,  $L = 0.01 \text{ H}$ , the simulation results are shown in Fig. 4.

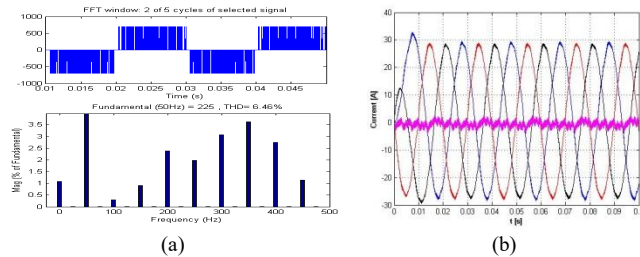


Fig. 4 (a) Phase A output voltage waveform and its FFT results  
(b) Three phase current and neutral current waveforms.

As shown in the Fig.4, the output voltage has a low THD (6.46%). Also the load currents are sinusoidal and the neutral current is almost zero.

Under the unbalanced load, the neutral current is handled with the LC output filter and the voltage error is compensated by the PI controllers based on the synchronous coordinates. The simulation results under unbalanced load condition are shown in

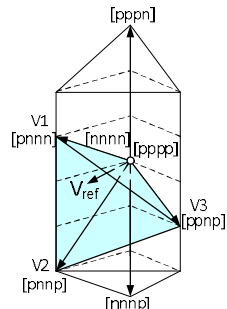


Fig. 3 Synthesis of the reference output vector.

Fig. 5 with the following load parameters: phase a,c:  $R = 10 \Omega$ ,  $L = 2\text{mH}$ , phase b:  $R = 5 \Omega$ ,  $L = 2\text{mH}$ ; LC output filter parameters:  $L = 660 \mu\text{H}$ ,  $C = 220 \mu\text{F}$ ,  $L_n = 330 \mu\text{H}$  on the neutral wire; and PI controller parameters:  $K_P = 9.7e-5$ ,  $K_I = 0.16$  on d, q channel and  $K_P = 6.5e-5$ ,  $K_I = 0.08$  on 0 channel.

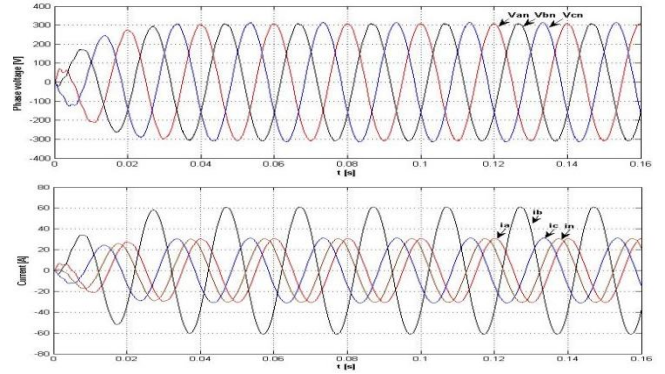


Fig. 5 Output voltage and current waveforms under unbalanced load.

As shown in the Fig. 5, the sinusoidal output voltages can be achieved under the unbalanced load condition with the system. In this case the neutral current is not equal to zero. Since, however, it is handled by the fourth leg, the zero-sequence current does not flow into the DC link capacitor and thus its capacitance value can be reduced significantly in this system.

An experimental prototype is built to verify the 3D SVM method. The 3D SVM algorithm is implemented on a DSP F2812, the PWM is performed by using Cyclone II 2C35 FPGA on the DE2 board from Altera. The experimental results are shown in Fig.6 under balanced load condition with following parameters:  $V_{in} = 110 V_{DC}$ ,  $M = 0.77$ ,  $f_{out} = 50\text{Hz}$ , the three-phase balanced load is a 3kW induction motor. Fig.6 shows the phase voltage waveforms and the vector diagram of the three phase outputs.

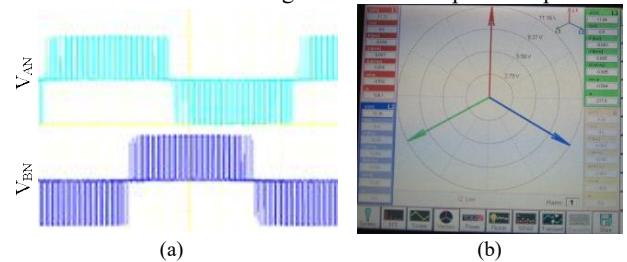


Fig. 6 (a) Output voltage waveforms (2.5 ms/div, 22V/div)  
(b) Output voltage vectors

#### 5. Conclusion

In this paper, the three dimensional space vector modulation method is applied for three phase four leg inverter system. With 3D SVM method, the three-phase four-leg topology can achieve higher modulation index, smaller DC-link capacitance and lower output distortion under unbalanced load condition. The system is suitable for the applications requiring high quality output under the unbalanced load condition.

#### References

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