변형 SL-ZSI의 설계 및 제어

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Design and Control of Modified Switched Inductor-ZSI

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ABSTRACT

This paper proposes a new topology with active switched-capacitor and switched-inductor impedance network, which can obtain a high boost factor with small shoot-through time. The proposed topology uses an active switched capacitor and switched-inductor impedance network in order to couple the main circuit and input dc source for boosting the output voltage. The proposed topology contains all advantages of the classical Z-source inverter. Comparing with other topologies, the proposed topology uses lesser component and the voltage boost inversion ability significantly increases. The theoretical analysis, pulse width modulation control strategies, and a comparison with classical ZSI have been given in this paper. Both simulation and experimental results will be presented to verify the advantages of the proposed topology.

1. INTRODUCTION

Nowadays, single-stage topologies are becoming the more t attractive subject compared with a three-phase inverter with a dc–dc boost converter. Among them, Z-source inverter (ZSI) was proposed [1]. Its advantage is a single-stage power conversion with buck-boost abilities, improving reliability without dead time and reducing the output waveform distortion. Recently, many enhanced dc-dc conversion techniques have proposed like switched-capacitor (SC), switched-inductor (SL), hybrid SC/SL, voltage multiplier cells [2], [3], which are used to get the high step-up capacity in transformerless and cascade structures. The main feature is to obtain a high efficiency, high power density, and simple structures. Thus, some successful combinations of the classical ZSI with SL (SL-ZSI) [4] or qZSI with SL (SL-qZSI) [5] have been made a good solution for improving the boost ability.

In this paper, a new topology is proposed. This topology is fully different with any other existing boost topology both the operation principle and structure. The main features of proposed topology can be summarized in the following: a new topology with active SC and SL impedance network, the bus voltage can boost by using the shoot-through states, the boost factor can increase by increasing the number of SL cell. The proposed inverter can improve by the coupled inductor solution. The simulation and experimental results are carried out to validate the proposed topology.

2. CIRCUITS ANALYSIS OF THE PROPOSED TOPOLOGY

The proposed topology is shown in Fig. 1. The switched impedance network consists of two inductors (L_1 and L_2), one capacitor (C) and five diodes (D_{in}, D_1, D_2, D_3, and D_0) and an active switch (S_7). The combination of L_1 - L_2 - D_1 - D_2 - D_3 produces the function of switched inductor cell, This SL cell is used to transfer and store energy from the capacitors to the dc–link voltage bus by the switching actions of the inverters.

The operating principle of the proposed topology is simplified with two states: shoot-through states and non-shoot-through states (active states and zero states) as shown in Fig. 2.

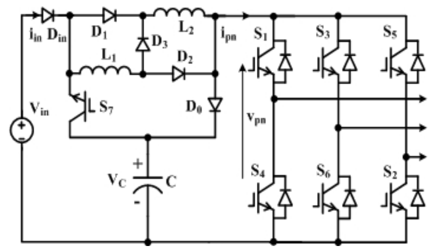

Fig. 1 Shematic of the proposed topology

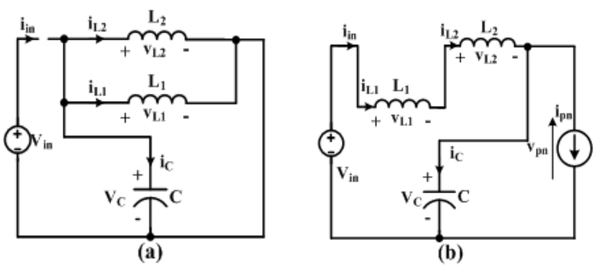

Fig. 2 Equivalent circuit: (a) shoot-through state. (b) non-shoot-through state.

The peak dc-link voltage across the inverter bridge is equal to V_C

$$\hat{v}_{pn} = V_C = \frac{1-D}{1-3D}.V_{in} = B.V_{in} \tag{1}$$

where B is boost factor of the proposed topology.

$$B = \frac{1-D}{1-3D} \tag{2}$$

Thus, the output peak phase voltage from the inverter can be expressed as follows:

$$\hat{v}_{ph} = M.\frac{\hat{v}_{pn}}{2} = M.B.\frac{V_{in}}{2} \tag{3}$$

where M is a modulation index.

The output ac voltage can step up or down by choosing an appropriate voltage gain G which is defined by M and B.

$$G = M.B \tag{4}$$

The obtainable output voltage is able to adjust in a wide range by regulating G. The boost factor B as expressed in (2) can be controlled by duty ratio D. Note that the shoot-through state does not affect the PWM control, because it is limited to the zero states which is determined by M.

In order to compare the boost ability with other topologies, the curves of the boost factor B versus the duty ratio D are plotted in Fig. 3. As shown in the Fig. 3, the boost ability of the proposed topology is stronger than a classical ZSI at the same operation condition.

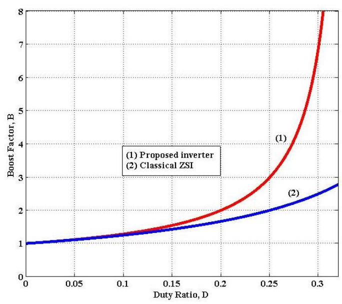

Fig. 3 Comparison of the boost factor with the classical ZSI.

3. SIMULATION AND EXPERMETAL RESULTS

A simulation is performed in the PSIM software in order to for verify the voltage boosting ability from the input voltage 40V and the output line-to-line voltage 120 V_{rms}. Here, the carrier-PWM control method is applied for the system. The simulation parameters are: $L_1 = L_2 = 1$ mH, C = 1000 µF, L_f = 600 µF, C_f =100 Hz, and resistive load R_L = 20 Ω/phase, the switch-ing frequency f_s = 5 kHz.

3-1. Simulation Results

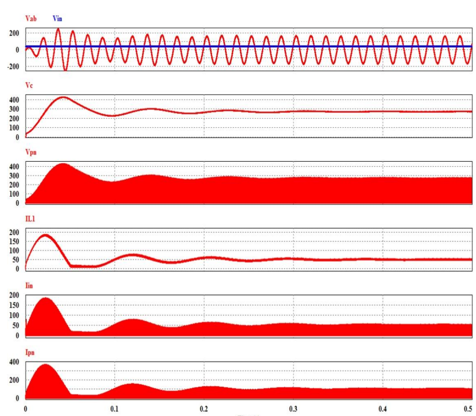

Fig. 4 Simulation results under the proposed PWM control method.

Fig. 4 shows the simulation results from the zero initial condition to the steady state, where V_{in}, V_{ab} (i.e., line-to-line output voltage), V_c, V_{pn}, i_{L1}, i_{in}, and i_{pn} are recorded, respectively. It is seen that the steady-state performance in the simulation is identically matching to the theoretical analysis.

3-2. Experimental Results

The experimental results under the condition of the proposed boost control method when modulation index M = 0.7 and duty ratio D = 0.3 is shown in Fig. 5. Fig. 5 shows the waveforms of the line-to-line voltage V_{ab}, output current I_a, capacitor voltage V_c, and input voltage V_{in} at the steady-state condition. In can been that the capacitor voltage is boosted to 260 V, and the peak of the inverter output voltage is about 120 Vrms.

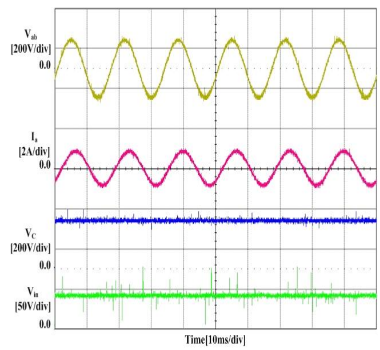

Fig. 5 Experiments results under the proposed boost control method when M = 0.7, D = 0.3, V_{in} = 40V.

4. CONCLUSION

In this paper, a new topology has proposed with improving performance compared with other topologies. The proposed inverter employs a active switched impedance network to couple the low dc voltage energy source to the main circuit of the inverter. By a detailed analysis, it is shown that the proposed inverter can provide the strong boost inversion ability. To illustrate the theoretical analysis, a case simulation for 40 V dc input and 120 V_{rms} line-to-line output voltage is given under the proposed boost control method. Both the simulation and experimental results present to confirm the advantages of the proposed topology. Therefore, the use of the proposed inverter can reduce the size and cost of the power converter in the applications of power electronics.

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