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Temperature Effect on the Interface Trap in Silicon Nanowire Pseudo-MOSFETs

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According to shrinkage of transistor, interface traps have been recognized as a major factor which limits the process development in manufacturing industry. The traps occur through spontaneous generation process, and spread into the forbidden band. There is a large change of current though a few traps are existed at the Si-SiO2 interface. Moreover, the increased temperature largely affects to the leakage current due to the interface trap. For this reason, we made an effort to find out the relationship between temperature and interface trap. The subthreshold swing (SS) was investigated to confirm the correlation. The simulated results show that the sphere of influence of trap is enlarged according to increase in temperature. To investigate the relationship between thermal energy and surface potential, we extracted the average surface potential and thermal energy (kT) according to the temperature. Despite an error rate of 6.5%, change rates of both thermal energy and average surface potential resemble each other in many ways. This allows that SS is affected by the trap within the range of the thermal energy from the surface energy.

Keywords: Interface trap, Pseudo-MOSFET, Silicon nanowire