

Si-nanoplate Transistors for Flexible Electronics

Mincheol Kim, Jungkyu Han

Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST),
Daejeon, 305-701, Republic of Korea
e-mail: bign@kaist.ac.kr

Sub 10-nm thick of Si plate is simulated with the software for Nanowire Field Effect Transistor (FET) device simulation. With usual single crystal Si technology, it is difficult to realize flexible electronic devices. Here, we suggest a FET device based on thinned Si layer. The simulation implied a practical limitation of the Si plate thickness for flexible devices as 2 nm. With around this thickness, Si plate may have much flexibility than existing bulk MOSFETs.

INTRODUCTION

Si based technology has witnessed its prosperous time for last decades. However, it was commonly known that its high-temperature process and its rigidity introduce a limitation in using it for flexible electronics. Nevertheless, recent reports [1] indicate that flexible electronics using well established Si technology may still be possible with the technology based on thinned Si layer. This work explores the electronic properties of transistors with ultrathin Si the thickness of which is reduced down to a nanometric scale.

METHODS

Ultrathin Si body tri-gate transistors were simulated with the software for Nanowire Field Effect Transistor (FET) device simulation from Edison-Nanophysics. In these devices, channels were formed using single crystal silicon plates in in various thicknesses, and the simulation was performed as if they were nanowire FETs. Detail specifications for the simulations based on the guideline of the software are presented in the table shown below.

Table 1. Design specifications used for simulation.*

Device Type	MOSFET	Channel Doping Type	i
Temperature	300	L source drain	10
Channel Material	Si	L channel	10

Oxide Material	SiO ₂	L gate	10
Valley	Delta	Mesh size transport direction	0.2
MI	0.92	T channel	Variable
Mt	0.19	W channel	3
Bandgap	1.21	T ox	1
Dielectric const. Channel	11.9	W ox	1
Bandgap Oxide	9	Mesh size confinement direction	0.1
Dielectric const. Oxide	3.9	Gate Configuration	Tri
Source Schottky Barrier Height	0.2	Sweep Voltage	Vg
Drain Schottky Barrier Height	0.2	Fixed Voltage	0.5
Transport Direction	100	Sweep From	0.3
x	[1 0 0]	Sweep To	1.4
y	[0 1 0]	Sweep increment	0.1
z	[0 0 1]		

RESULTS

It is highly recommended to use this style as is for preparing your abstract. It is fine to tweak the margins a little, just bear in mind the abstracts will be bound in a book. Abstracts severely violating the suggested format will be treated as regular submissions and reviewed but might be excluded from the Book of Abstracts.

DISCUSSION

As the thickness of the single crystal Si plate decreases, the on current level severely decreases. There is, however, a negligible change in drain current divided by the thickness of Si-plate, until the thickness of Si plate becomes less than 2 nm [Fig. 1.]. This implies that the main reason of decrease in drain current of Si-plate transistors is the decrease of Si-plate. With the thickness under 2 nm, devices require a larger gate bias to achieve the same amount of the drain current divided by the thickness of Si-plate. It seems the deficiency in the number of carriers within ultrathin Si-plate becomes the limiting factor for the drain current. This explanation seems feasible when the lattice constant of the single crystal silicon is considered. Through the simple relation with the diamond structure and the lattice constant of single crystal silicon, the size of Si atom can be roughly estimated as 2.35 Å [2].

CONCLUSION

Simulated results suggest a practical limitation of the thickness for flexible transistors as 2 nm. With around this thickness, Si plate may have much flexibility than bulk type of existing MOSFETs. As for applications for these flexible sensors, one may imagine an artificial vascular system equipped with chemical sensors and manometers based on such ultrathin Si-plate transistors [Fig. 2.].

REFERENCES

- [1] E. Menard et al., Applied Physics Letters **86**, 093507 (2005).
- [2] Donald A. Neamen, Semiconductor Physics and Devices; Basic Principles, **Third Edition**, McGraw-Hill Education (2003).

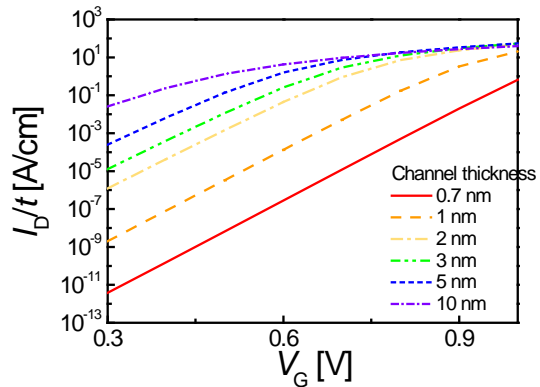


Fig. 1. Simulated V_G vs. drain current divided by the thickness of Si-plate

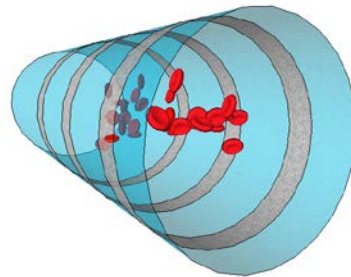


Fig. 2. An imaginary picture of an artificial vascular system using band-like Si-plate transistors