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Copper Interconnection and Flip Chip Packaging Laboratory Activity for Microelectronics Manufacturing Engineers

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In the era of 20 nm scaled semiconductor volume manufacturing, Microelectronics Manufacturing Engineering Education is presented in this paper. The purpose of microelectronic engineering education is to educate engineers to work in the semiconductor industry; it is therefore should be considered even before than technology development. Three Microelectronics Manufacturing Engineering related courses are introduced, and how undergraduate students acquired hands-on experience on Microelectronics fabrication and manufacturing. Conventionally employed wire bonding was recognized as not only an additional parasitic source in high-frequency mobile applications due to the increased inductance caused from the wiring loop, but also a huddle for minimizing IC packaging footprint. To alleviate the concerns, chip bumping technologies such as flip chip bumping and pillar bumping have been suggested as promising chip assembly methods to provide high-density interconnects and lower signal propagation delay [1,2]. Aluminum as metal interconnecting material over the decades in integrated circuits (ICs) manufacturing has been rapidly replaced with copper in majority IC products. A single copper metal layer with various test patterns of lines and vias and 400 μm by 400 μm interconnected pads are formed. Mask M1 allows metal interconnection patterns on 4” wafers with AZ1512 positive tone photoresist, and Cu/TiN/Ti layers are wet etched in two steps. We employed WPR, a thick patternable negative photoresist, manufactured by JSR Corp., which is specifically developed as dielectric material for multi- chip packaging (MCP) and package-on-package (PoP). Spin-coating at 1,000 rpm, i-line UV exposure, and 1 hour curing at 110°C allows about 25 μm thick passivation layer before performing wafer level soldering. Conventional Si3N4 passivation between Cu and WPR layer using plasma CVD can be an optional. To practice the board level flip chip assembly, individual students draw their own fan-outs of 40 rectangle pads using Eagle CAD, a free PCB artwork EDA. Individuals then transfer the test circuitry on a blank CCFL board followed by Cu etching and solder mask processes. Negative dry film resist (DFR), Accimage®, manufactured

by Kolon Industries, Inc., was used for solder resist for ball grid array (BGA). We demonstrated how Microelectronics Manufacturing Engineering education has been performed by presenting brief intermediate by-product from undergraduate and graduate students. Microelectronics Manufacturing Engineering, once again, is to educating engineers to actively work in the area of semiconductor manufacturing. Through one semester senior level hands-on laboratory course, participating students will have clearer understanding on microelectronics manufacturing and realized the importance of manufacturing yield in practice.

Keywords: Copper Interconnect, Flip Chip packaging, Microelectronics Manufacturing Education