Testing and Self Calibration of RF Circuit using MEMS Switches

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Abstract

This paper presents testing and self-calibration of RF circuits using MEMS switches to identify process-related defects and out of specification circuits. We have developed a novel multi-tone dither test technique where the test stimulus is generated by modulating the RF carrier signal with a multi-tone signal generated using an Arbitrary Waveform Generator (AWG) with additive white Gaussian noise. This test stimulus is provided as input to the RF circuit and peak-to-average ratio (PAR) is measured at the output. For a faulty circuit, a significant difference is observed in the value of PAR as compared to a fault-free circuit. Simulation is performed for various circuit conditions such as fault-free as well as fault-induced and their corresponding PARs are stored in the look-up table. This testing and self-calibration technique is exhaustive and efficient for present-day communication systems.

I. Introduction

Modern day communication systems require the presence of the entire radio frequency (RF) system on a single chip. CMOS technology is widely considered for designing the RF system as it provides the advantage of high functionality at low cost. However, as the CMOS technology shrinks to nanometer dimensions, the sensitivity of process variations causes degradation in the RF performance of the circuit. This makes designing sensitive RF circuits extremely difficult. Also, the extraction of parasitics of the passive devices becomes increasingly difficult due to the higher operating frequencies and smaller interconnects spacing. These problems lead to a significant loss in parametric yield. Hence, testing the fabricated chip for parametric variations becomes very essential.

Once the chip is packaged to realize the device, with constant usage over a continuous period of time there is a high probability of performance variations occurring within the chip[1-3]. These variations are attributed to thermal fatigue, mechanical shock, self-heating, electro-migration, etc. In present day consumer electronics, a device is guaranteed to work over a specific period of time. But replacing RF chips that exhibit low performance after continuous usage due to various fatigues and ageing factors is not cost effective. Hence, it is of the utmost importance to automatically detect the performance variations within the device and self-calibrate it to design specification levels. A self-calibration methodology that can address both process and time-degraded variations is presented in this paper.

We propose a System-on Chip (SoC) approach to design the RF, testing and self-calibration circuits on a single chip. Our tuning circuit used for self-calibration is based on MEMS switches and this increases the complexity of fabricating multiple technologies on a single silicon substrate. To overcome this, we have designed them on different dies and stacked these dies together using through silicon via (TSV) technology. Fig. 1 shows the internal block diagram of the proposed testing and self-calibration approach.

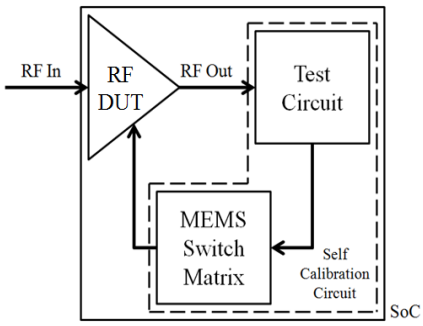

Figure 1: System-on-Chip Architecture of the Test and Self-calibration Circuitry.

II. LNA Design and Test Stimulus Synthesis

In conventional communication systems, the RF front-end receiver has different functional blocks. Among these, the most important block is the LNA. LNA is generally the first stage of the RF receiver sub-system, and its functional performance is very essential as it amplifies the received low power signal by the designed amplification factor to be given to the next stage. Ideally an LNA suppresses externally acquired noise and amplifies the input signal. But, in practical applications, the LNA reduces the input signal noise and adds an extremely low noise to the input signal [4]. Hence, designing LNA is crictical and painstaking.

A narrowband LNA (N-LNA) is used as the reference RF circuit in this paper. The design requirements of the LNA focus on high gain, low noise, stability, high linearity, perfect input-output match and low power consumption. Impedance matching is one of the most important factors considered during LNA design. The input reflection coefficient (S_{11}) determines the input match and it also relates to the forward gain (S_{21}) of the LNA.

Parametric variations cause a shift in the operating frequency of the LNA thereby, leading to a change in S_{11} and S_{21} parameters[5]. This leads to an impedance mismatch between the LNA and the following stages of the RF receiver resulting in attenuation of input signal. Designing an LNA, especially for high frequency applications, is challenging to even the most experienced circuit designers for the following reasons [6].

1. Selection of Transistor, which is the first and most important step in the LNA design.
2. Too many factors to be considered simultaneously - high gain, low noise figure, unconditional stability and good input and output match at the lowest possible current levels.
3. Design challenges such as Interdependence of gain, stability, noise figure and input/output match.

In this paper, the Atmel n-channel MOSFET based on 0.18μm CMOS technology was chosen as the transistor for designing the LNA. The specifications of the LNA are listed in Table 1.

Table 1: LNA Specifications

Parameter	Symbol	Range
Input Match	S_{11}	≤ -15 dB
Forward Gain	S_{21}	≥ 8 dB
Output Match	S_{22}	≤ -10 dB
Noise Figure	NF	≤ 2 dB
Stability Factor	K	≥ 1

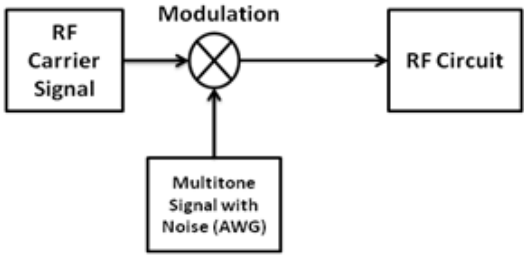

Figure 2: Test Signal Synthesis [8]

This test signal is obtained by maintaining the frequency of the RF carrier signal and the multi-tone signal at the same level. Fig. 3 shows the test signal in frequency domain.

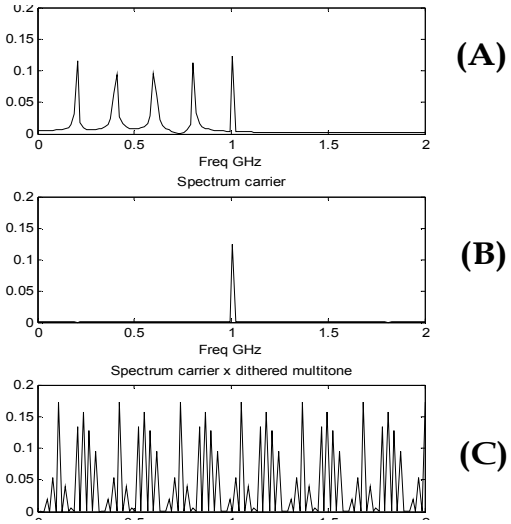

Figure 3: Input Test Signal for Dither Testing: (A) Multi-tone Signal, (B) RF Carrier Signal, (C) Multi-tone Signal Modulated with the RF Carrier Signal [8]

The test signal is provided as input stimulus to the LNA and the output of LNA is given to a detector which records the peak and average values to obtain the PAR values. For a perfectly matched LNA, there are a set of values defined for the components in the circuit like the gate capacitance (C_g), source inductance (L_s), drain capacitance(C_d), etc. If these values are disturbed, the parameters of the LNA drift away from their designed values. Simulation was performed and the PAR values were observed for several fault inducted cases. There is a significant

difference in the PAR values between the fault free and the fault induced cases. Besides, we can identify a significant difference in PAR values for individual faults and multiple faults. This allowed us to identify the specific defect(s) with a high precision. Once the defect is identified we perform calibration using MEMS tuning circuit discussed in the following section.

III. MEMS Tuning Circuit

The proposed self-calibration scheme consists of a tuning circuit which is interfaced with the LNA by MEMS switches. The tuning circuit consists of a bank of inductors and a capacitor which is connected to the LNA such that the input and output impedance match is retained to design level specifications after calibration is performed. Fig. 4 shows the LNA circuit schematic with the MEMS tuning circuit.

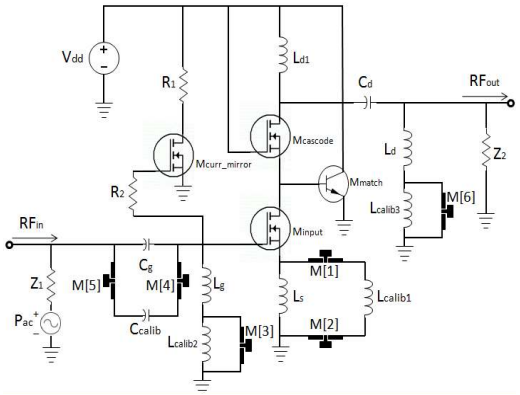

Figure 4: LNA with MEMS Tuning Circuit.

In the figure shown above M[1], M[2], M[3], M[4], M[5], M[6] represent the MEMS switches and L_{calib1}, L_{calib2}, L_{calib3} and C_{calib} represent the additional tuning circuit components used for self-calibration respectively. Check 1 to 1 matching The values of L_{calib1}, L_{calib2}, L_{calib3} and C_{calib} are determined by taking into account the sensitivity level of the respective component they calibrate. Since, these tuning components are fabricated on the die and their parametric values are non-scalable we perform LNA calibration up to a predetermined range. The values of L_{calib1}, L_{calib2}, L_{calib3} and C_{calib} are obtained by using the equations shown below with the design constraint being that the input and output match should not be disturbed.

$$L_{calib1}=\frac{3L_s}{2} \quad (1) \qquad L_{calib2}=\frac{L_g}{2} \quad (2)$$

$$L_{calib3}=\frac{L_d}{2} \quad (3) \qquad C_{calib}=\frac{14C_g}{5} \quad (4)$$

To perform calibration, the MEMS switches are either turned ON or OFF to interface respective tuning circuit components to the LNA. The LNA is initially tested for fault-free case and later by inducing faults in various components using the multi-tone dither test technique, the PAR values for each respective case is recorded and stored in a look-up table. By comparing the PAR value of fault-free case to the fault-induced case we localize the fault to a respective component in the LNA circuit. Once the fault is localized this information is carried over to determine which MEMS switches are activated by the MEMS switch matrix. The MEMS switch matrix is a (1x6) matrix with '0' representing OFF state and '1' representing ON state of the MEMS switches. The syntax of the MEMS switch matrix is M[1,i] where i = 1,2,..,6 representing individual MEMS switches. Table 2 shows the look-up table with the MEMS switch matrix.

Table 2: Look-up Table

Condition	Sensitivity	Differential PAR	MEMS Switch Matrix
Fault-free	None	0	[0,0,0,0,0,0]
C_g	20% decrease	16.2	[0,0,0,1,1,0]
L_g	30% decrease	8.3	[0,0,1,0,0,0]

In the case of a faulty LNA, the MEMS switches to be activated to perform calibration are determined from the differential PAR values. If a MEMS switch is activated, a "1" which is equivalent to 9V is stored; else a "0" which is equivalent to 0V is stored in the switch matrix respectively.

IV. LNA Testing - Simulation Results

LNA testing is performed using the multi-tone dither test technique. The synthesized test stimulus is given as input signal to the LNA and the corresponding output PAR is computed using the following relations [7].

$$P.A.R=\frac{V_{peak}}{V_{rms}} \quad (5)$$

$$V_{peak}=\max_t\{|a(t)|\} \quad (6)$$

$$V_{rms}=\sqrt{\lim_{x\to N}\frac{1}{2x}\int_0^N a^2(t)dt} \quad (7)$$

The sensitivity of test depends on the test frequency and the number of tones used. The PAR values computed are stored in the look-up table shown above. When fault-free simulation is completed we induce different faults in the LNA and perform exhaustive fault condition simulations and record the PAR values in the look-up table. Hardware testing of the LNA is performed after the look-up table is populated and the output is compared with the look-up table to identify the LNA functional performance level. If the LNA is faulty then based on the MEMS switch matrix we activate the respective MEMS switches to perform calibration.

In this case the gate capacitor, C_g. is varied from design level specifications of the LNA. This affects the parametric yield of the LNA. If a fault is induced into the LNA at C_g by reducing it by 40%, then the resultant gain and noise figure are as shown in Fig. 5(a,b).

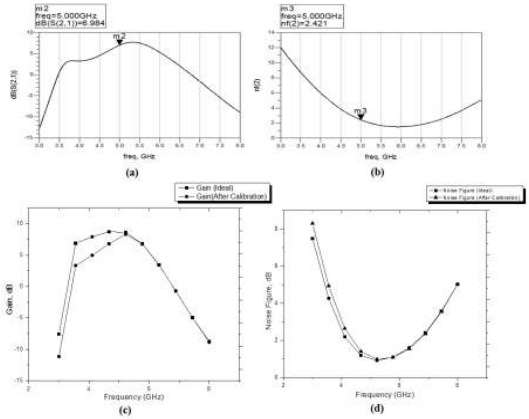

Figure 5: (a) Transmission Coefficient, (b) Noise Figure, (c) Gain – Fault Free vs. Calibrated, (d) Noise Figure – Fault Free vs. Calibrated.

Gain is reduced to 6.98dB from 8.9dB and the noise figure is increased to 2.44dB from 0.96dB. By following the testing procedure mentioned in section 3, the respective MEMS switch matrix chosen is [0, 0, 0, 1, 1, 0]. From the switch matrix it is seen that the switches M[4] and M[5] are activated. The gain response after calibration is compared with the fault-free LNA is shown in Fig. 5(c) and the noise figure after calibration compared to fault-free LNA is shown in Fig. 5(d).

V. Conclusion

A novel testing and self-calibration scheme has been presented in this paper. These schemes are integrated with the designed 5 GHz LNA on a single chip and help in improving its performance over process variations. The test circuitry includes an envelope detector to compute the PAR values of the RF output of the LNA. The PAR values are digitized by the ADC and the result is compared with the look-up table stored in the DSP to test the LNA. Faulty LNAs are calibrated by generating MEMS switch matrix from the look-up table.

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