Digital Active Load Sharing Control of Paralleled Phase-Shifted Full-Bridge Converters

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Abstract

For the high power demand and N+1 redundancy, this paper presents the digital load share (LS) controller design and the implementation of paralleled phase-shifted full-bridge converters (PSFBC) used in distributed power systems. By adopting the digital control strategy, separately used ICs for PSFBC and LS control functions in analog systems can be merged into a cost-effective digital controller. To compensate and stabilize both PSFBC and LS loops with the direct digital design approaches, small-signal model of the system is derived in discrete-time domain. The steady-state and dynamic load sharing performances are also investigated. Experimental results from two 1.2 kW paralleled PSFBC modules are shown to verify the proposed work.

1. Introduction

Distributed power systems such as server and network systems need high-current capacity, high efficiency, high maintainability, high reliability, etc [1]. To meet these requirements, the paralleled phase-shifted full-bridge converter (PSFBC) with an equally distributed load current will be one of the most suitable candidates especially in high power applications. By sharing the load current equally in each modularized PSFBC, the system can maximize reliability, improve the operational redundancy, and reduce the cost of maintenance [2]. However, separate ICs for the PSFBC control and the load share (LS) control should be utilized.

Recently, digitally controlled DC-DC converters seem to be of growing interest in many industries due to the high-speed computing processor and variously provided peripherals such as PWM modules, A/D converter (ADC) modules, and several external interfaces. Since most of the micro-controller units (MCUs) or digital signal processors (DSPs) offer the sufficient number of PWM and ADC modules, it is possible to control the PSFBC and LS simultaneously with one MCU. Moreover, easy modifications and real-time monitoring of control parameters can lead to ease of the realization and the reduction of the development time.

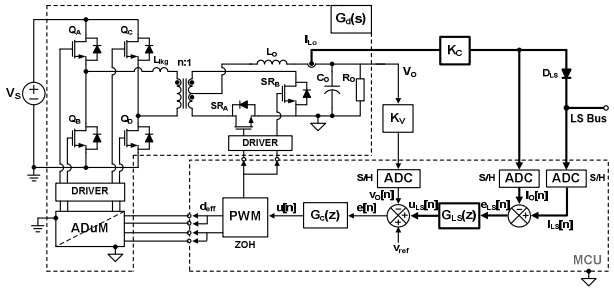

Fig. 1. Digital load sharing control block of a modularized PSFBC.

The previous efforts to equalize the modules inductor currents are presented in the literatures [3]-[5]. Among all these control methods, the active LS control method, with a load share bus carrying a reference current signal, is more accurate than the passive droop method [6]. However, not only the discrete-time domain analysis for the active LS control method but also the modularized PSFBC as the paralleled DC-DC converter have not been introduced so far. Therefore, to cope with a high power demand and achieve an accurate current balance, the digitally controlled PSFBC using active LS control method is presented in this paper.

Prior to design a digital LS controller, the voltage-mode controller design of PSFBC is described in section 2. In section 3, based on the designed PSFBC digital controller, small-signal model of LS loop in the discrete-time domain is derived and then compensated. After that, experimental results are presented in section 4. Finally section 5 reaches a conclusion.

2. Digital Voltage-Mode Control of PSFBC

Fig. 1 describes the digital LS control block diagram of the paralleled PSFBC. It consists of both an inner voltage-mode PSFBC control loop and an outer LS loop employing an LS diode, D_{LS}. The effective duty-to-output transfer function of PSFBC, $G_d(s)$, can be derived from the averaged small-signal model considering the change of the duty ratio caused by the output inductor current I_{LO} and the input voltage V_S [7]. It can be expressed as (1) which is well presented in [7].

$$G_d(s) = \frac{\hat{v_O}}{\hat{d_{eff}}} = \frac{nV_S}{L_O C_O} \frac{1}{s^2 + s(\frac{1}{R_O C_O} + \frac{R_d}{L_O}) + \frac{1}{L_O C_O}(1 + \frac{R_d}{R_O})} \quad (1)$$

, where $R_d = 4n^2 L_{lkg} f_s$. L_{lkg} and f_s are denoted by the transformer leakage inductance and the switching frequency respectively. By considering both the sample-and-hold (S/H) effect and the computation delay, the discrete-time transfer function of PSFBC can be expressed as (2). That is, $G_d(z)$ contains the impulse sampler, the zero-order hold (ZOH), and the time delay function led from the one-cycle delayed control.

$$G_d(z) = \mathbf{Z}\{\frac{1 - e^{-sT_S}}{s} \cdot e^{-sT_d} \cdot G_d(s)\} \quad (2)$$

$Z\{*\}$ denotes z-transformation of *, where T_S and T_d indicate the sampling period and the computation time-delay respectively. The voltage feedback control loop of the PSFBC, $T_V(z)$, can be easily derived as (3) including voltage sensing gain K_V and the PSFBC controller $G_C(z)$.

$$T_V(z) = K_V \cdot G_d(z) \cdot G_C(z) \quad (3)$$

$$G_C(z) = \frac{u[n]}{e[n]} = K_P \frac{(z - z_1)(z - z_2)(z - z_3)}{(z - 1)z^2} \quad (4)$$

The PSFBC controller $G_C(z)$ expressed in (4) is designed as 1-integrator for the infinite DC gain, 2-high frequency pole so as to ensure the maximum phase margin, and 3-zero which compensates

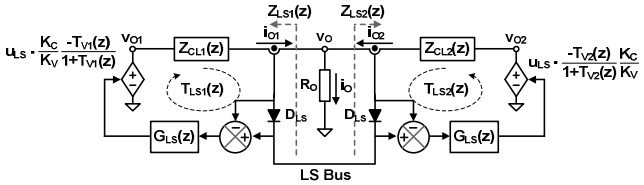

Fig. 2. Active load sharing model of two paralleled PSFBCs.

the phase delays due to the 2-pole in $G_d(z)$ and 1-integrator in $G_C(z)$. Besides, extra phase delays due to ZOH and T_d included in $G_d(z)$ are considered for the design accuracy. Based on the designed PSFBC controller $G_C(z)$, the digital LS controller $G_{LS}(z)$ design will be presented in the following section.

3. Digital Active Load Sharing Control of PSFBCs

To derive the LS control loop, the small-signal model of two paralleled PSFBCs using the output impedance concept is described in Fig. 2, The system consists of the modified controlled voltage source, the closed-loop output impedance $Z_{CL}(z)$, the output current sensing gain K_C, and the LS controller $G_{LS}(z)$. $Z_{CL}(z)$ for the PSFBC can be expressed as (5) by using the step invariant discretization method.

$$Z_{OL}(z)=\mathbf{Z}\{(\frac{1-e^{-sT_S}}{s})(\frac{sL_O}{s^2L_OC_O+s\frac{L_O}{R_O}+1}+\frac{1}{(s^2L_OC_O+s\frac{L_O}{R_O}+1)^2}\cdot\frac{1}{\frac{1+sR_OC_O}{s^2R_OL_OC_O+sL_O+R_O}+\frac{1}{R_d}})\}$$

$$Z_{CL}(z)=\frac{Z_{OL}(z)}{1+T_V(z)} \quad (5)$$

In the active load sharing method using the LS diode D_{LS}, the paralleled module having the highest current gives the conduction of D_{LS}. It means only one master unit communicates on the LS bus and the other slave modules adjust the reference voltage accordingly to correct the imbalance of load current. Because of no LS error from the master position, the LS feedback control loop $T_{LS}(z)$ in the slave position is a matter of concern. Thus, the LS feedback control loop $T_{LS}(z)$ can be derived as (6).

$$T_{LS}(z)=\frac{K_C}{K_V}\cdot\frac{T_V(z)}{1+T_V(z)}\cdot\frac{1}{Z_{CL}(z)}\cdot G_{LS}(z)=\frac{K_C}{K_V}\cdot\frac{T_V(z)}{Z_{OL}(z)}\cdot G_{LS}(z) \quad (6)$$

Fig. 3 shows the bode plot of the discrete-time PSFBC LS systems. Equation (7) is the designed LS controller which consists of 1-integrator to assure no steady-state LS error, 1-low frequency zero to compensate the phase delay, and 1-pole to alleviate the high frequency ripples. The closed loop bandwidth is allocated at 300Hz with a phase margin of 70°. Since the dynamic characteristics of the LS system depend on the LS loop bandwidth and its phase margin, the trade-off between the bandwidth and the stability issue should be considered.

$$G_{LS}(z)=\frac{u_{LS}[n]}{e_{LS}[n]}=K_{LS}\frac{(z-z_{LS1})}{(z-1)(z-p_{LS1})} \quad (7)$$

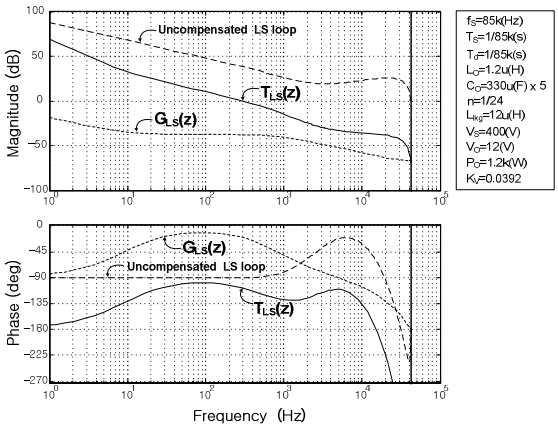

Fig. 3. Bode Plot of the discrete-time PSFBC LS systems.

4. Experimental Results

To verify the analysis and validity of the designed digital LS controller, two identical 1.2kW PSFBC modules have been built, where the system and design parameters are noted in Fig. 3. The designed digital controllers, i.e. $G_C(z)$ and $G_{LS}(z)$, of each module are implemented on a TMS320F28027. It offers that 60MHz system clock, 8 channels for PWM, 13 channels for ADC, three 32-bit CPU timers, and so on. Table I. illustrates the steady-state LS errors according to the total load current variations. In spite of the additional phase delays due to the digitally controlled-loop, it can be concluded that the steady-state LS errors are nearly eliminated by an integrator in the LS controller. Fig. 4 shows the experimental waveforms for dynamic load currents from 5A to 100A and vice versa. The designed 2-pole and 1-zero LS controller makes each modular current be equal with a fast dynamics.

Table. I. Steady-state LS performance.

I_{O1} (A)	1.04	5.04	14.91	24.81	34.59	50.09
I_{O2} (A)	0.97	4.92	14.67	24.83	35.17	49.72
$I_O/2$ (A)	1.01	4.98	14.79	24.82	34.88	49.91
ΔI_O (A)	0.07	0.12	0.24	0.02	0.58	0.37
$\Delta I_O/(I_O/2)$ (%)	6.96	2.41	1.62	0.08	1.66	0.74

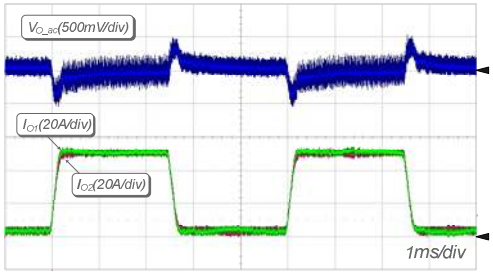

Fig. 4. Experimental waveform (5A→100A→5A).

5. Conclusion

This paper presented the digital LS controller design of paralleled PSFBC modules. The active LS control method using a LS bus with diodes was implemented. By the experimental results, ignorable steady-state errors and a fast dynamic response were achieved with a cost-effective digital controller.

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