스트레인드 채널이 무캐패시터 메모리 셀의 메모리 마진에 미치는 영향

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Impact of strained channel on the memory margin of Cap-less memory cell

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Abstract : We investigated the dependence of the memory margin of the Cap-less memory cell on the strain of top silicon channel layer and also compared kink effect of strained Cap-less memory cell with the conventional Cap-less memory cell. For comparison of the characteristic of the memory margin of Cap-less memory cell on the strain channel layer, Cap-less transistors were fabricated on fully depleted strained silicon-on-insulator of 0.73-% tensile strain and conventional silicon-on-insulator substrate. The thickness of channel layer was fabricated as 40 nm to obtain optimal memory margin. We obtained the enhancement of 2.12 times in the memory margin of Cap-less memory cell on strained-silicon-on-insulator substrate, compared with a conventional SOI substrate. In particular, much higher D1 current of Cap-less memory cell was observed, resulted from a higher drain conductance of 2.65 times at the kink region, induced by the 1.7 times higher electron mobility in the strain channel than the conventional Cap-less memory cell at the effective field of 0.3MV/cm. Enhancement of memory margin supports the strained Cap-less memory cell can be promising substrate structures to improve the characteristics of Cap-less memory cell.

Key Words : Cap-less memory cell, Strained SOI, SOI, memory margin, kink effect