New Plasma Etchant를 사용하여 Spacer dry etch 공정의 최적화

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Optimizing Spacer Dry Etch Process using New Plasma Etchant

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Abstract : We studied about the effect of newly developed etchant for spacer etch process in gate patterning. With the 110nm CMOS technology, first, we changed the gate pattern size and investigated the variation of spacer etch profile according to the difference in gate length. Second, thickness of spacer nitride was changed and effect of etchant on difference in nitride thickness was observed. In addition to these, spacer etch power was added as test item for variation of etch profile. We investigated the etch profiles with SEM and TEM analysis was used for plasma damage check. With these results we could check the process margins for gate patterning which could hold best performance and choose the condition for best spacer etch profile.