Highly integrated LCD bias and control IC

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Abstract

Each LCD TFT panel requires a power supply IC on the panel board. The IC provides the power rails for the timing controller, source and gated driver IC and others. The industry trend moves towards higher integrated devices. The challenge for the panel manufacturer is the development and implementation of such an IC in cooperation with the semiconductor supplier. If not done carefully the solution will not reduce the overall solution cost or can't provide the expected performance and reliability. This paper discusses the key considerations to successfully develop and integrate a highly integrated LCD bias IC into the system.

1. Introduction

A typical TFT LCD panel requires following voltage rails and functions.

1. Source Driver supply voltage (AVDD)
2. Gate Driver supply voltage (VGH and VGL)
3. Logic supply voltage (3.3V, 2.5V)
4. Half AVDD drive supply for source IC (HAVDD)
5. Vcom supply rail (One or more OpAmps)
6. Gate voltage modulation
7. Temperature compensation for VGH, VGL and or VCOM
8. Level shifter for gate in panel TFT technologies
9. Gamma correction
10. Sequencing and logic (Power good, reset, etc.)
11. Programming interface usually I2C compatible

All those voltage rails and functions are required to operate the panel. In the past such a system was typically built by using discrete components like boost converter, buck converter, charge pumps and so on. As the system gets more mature a fully integrated Compact LCD bias IC is taking care of all the functions and voltage rails. As a major goal an integrated IC should achieve a lower total solution cost compared to the discrete solution. The challenge is to develop such an integrated IC in cooperation with the IC manufacturer. For a successful development of an integrated IC following system requirements need to be considered.

1. Total solution cost
2. Power dissipation and efficiency
3. PCB board space and layout
4. System performance, functionality and reliability

The solution needs to fulfill those requirements best but could slightly vary from application to application. In the next section it is discussed how these requirements can be met and what are the trade-offs. Considering and understanding those requirements and the consequent trade-offs increases the success of developing and implementing a fully integrated IC for a TFT LCD panel.

2. Results and discussion

Total solution cost
When moving to an integrated compact LCD bias IC one of the main goals is to achieve lower total solution cost. This is only possible when the *right* functions are being integrated. Therefore it is wise to spend more time and resources to identify the *right* functions to be integrated in order to get the highest return of investment. The difficulty here is the identification of the *right* functions. In order to work out a guideline for integration we need to look at the split of the cost for package, silicon and other cost.

TABLE 1. LCD bias device cost

Package cost	25% to 60%
Silicon cost	30% to 60%
Other cost	10% to 20%

Other cost includes mainly test cost and yield. The variance of silicon cost and package cost depends on the process being used and package size and pin count. As a general rule the higher the pin count the larger the package cost. The silicon cost mainly depends on process, wafer cost and actual silicon size. Therefore it is not possible to provide an accurate split between package and silicon cost in general because they vary from IC supplier to IC supplier in a large extend. The importance here is that the package cost can be as high as 60% of the overall cost. A lower package pin count can significantly lower overall solution cost. When considering the functions and voltage rails to be integrated the pin count needs to be minimized compared to the discrete solution.
The other area to consider is the silicon size of the discrete solution versus an integrated solution. Any sequencing and control function which require usually several logic and analog discrete ICs, can typically be integrated at much lower cost. They require minimum silicon size but remove several external ICs. When integrating any power functions it is not always cheaper compared to a discrete solution and needs to be carefully considered in terms of power dissipation, voltage rating and required MOSFET on resistance. Integration of high voltage functions, like 20V and larger also increase the silicon cost and need to be carefully considered. As a general rule the lower the required voltage rating the lower the silicon cost.

Power Dissipation and Efficiency

The package temperature during operation should typically not exceed 70degC. This puts a clear limit to the converter and LCD bias design in terms of integration. The higher the level of integration the higher the operating temperature. A conventional TSSOP or QFN package can dissipate around 1.5W at 25°C ambient temperature. Figure 1 shows a typical LCD board operating at 25°C ambient temperature.

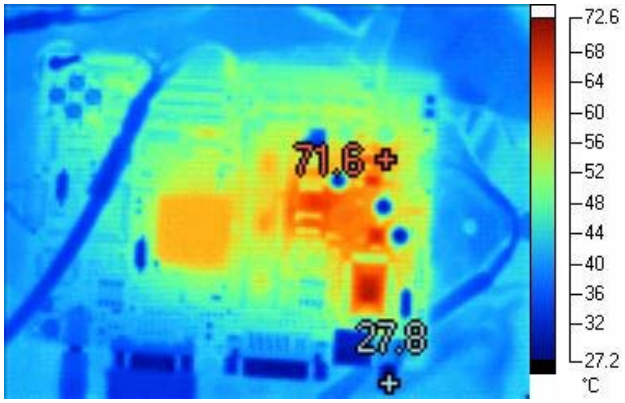

Fig. 1. Typical temperature distribution of a LCD panel board

In the example of Figure 1 some of the devices run already at 70°C. When mounting such a board on a LCD panel using CCFL backlight then the board temperature and IC temperature will further rise. Figure 1 also shows the high temperature being concentrated around a small area of the PCB while other areas are rather cool. To further reduce the IC temperature it is necessary moving the devices generating heat in colder areas of the PCB to achieve a more uniform temperature distribution. Due to this, the PCB layout has a major effect on IC temperature. With a fully integrated LCD bias IC, the generated heat is mainly concentrated on a single package. Therefore the level of integration is also limited by the power dissipation of the package. In order to achieve highest IC integration following steps need to be considered:

1. High converter efficiency
2. PCB temperature reduction by
   - LED backlight produces less heat compared to CCFL
   - Uniform temperature distribution by placing components and ICs across the PCB
   - PCB layout needs to be optimized for power dissipation using thermal vias and thermal planes

Board space and layout

The PCB is sometimes placed on the top side of the panel. Then the width of the PCB is limited to 18mm or less. Using a discrete solution allows to distribute each converter IC across the PCB. For high integrated solution the package dimension itself might become a problem already, when using a PCB with a minimum

width. Typically QFN packages are used for such applications due to the good thermal characteristics, small solution size, high pin count and moderate package costs. Such a package is also shown in Figure 2. As the integration and pin count increases the QFN package reaches its limits. Especially packages larger than 9x9mm may cause board level reliability problems and limit the possible PCB mechanical width. Because of this, the pin count of the solution should be kept to a minimum or alternative packages need to be used. At this point of time possible alternative packages usually increase the solution cost accordingly.
When more converter are integrated on one IC then the PCB layout becomes more and more difficult compared to the discrete solution. In particular this is a problem with large TFT LCD screens >37" when the converter currents are much higher.
Higher converter currents increase parasitic effects of the PCB board. This can cause un-desired interaction between the converter of the IC due to increased ground noise and voltage drops.

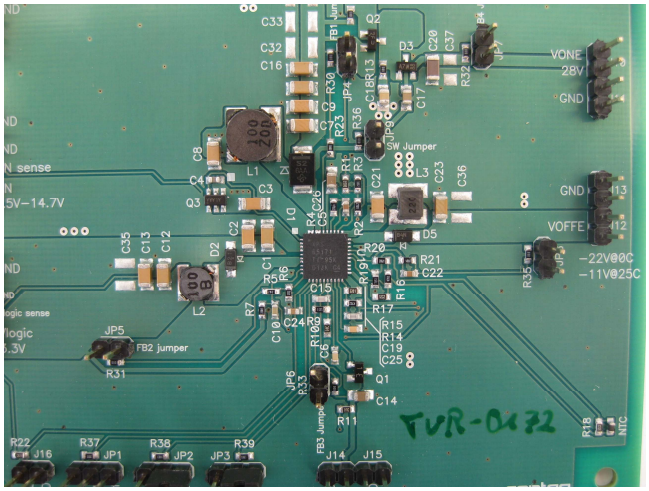

Fig. 2. Typical application board of a Compact LCD bias IC

Figure 2 shows such a typical PCB layout for a compact LCD bias IC. This converter contains a boost converter, buck converter, VGH and VGL supply, temperature compensation and sequencing control. The pin out and therefore the required PCB layout of the IC should support following items:

1. Simple layout for all supply and ground connection of each converter
2. Pin out should consider panel board layout and LCD connector placement
3. Handle pin to pin shortages
4. Pin count needs to be kept to a minimum

The simplicity of the PCB layout starts with the pin out of the IC and special care needs to be taken. The challenge for the IC supplier is to simplify the design as much as possible while the power integration constantly increases. Eventually the IC should be a plug and play solution. For today's applications the PCB layout is still a major task in achieving optimum device performance and requires engineering time that should be planned in accordingly.

System Performance, functionality and reliability

Today's systems are fairly complex. They require a good understanding of analog and power management circuits. Furthermore the interaction between LCD and power management and the necessary control circuit are of high importance. An optimized solution can only be achieved with a good understanding of the entire system. This includes the LCD technology as well as the power management and control technology. Shorter design cycle times and more complex LCD bias and control circuit make it difficult to understand the newest technology in a very detailed level. Historically a discrete solution is developed and implemented for new LCD technologies. Then the discrete functions are integrated in a single IC. However the discrete solution is not necessarily the best solution. For example more and more systems are using now the so called "Half AVDD" drive as shown in Figure 3.

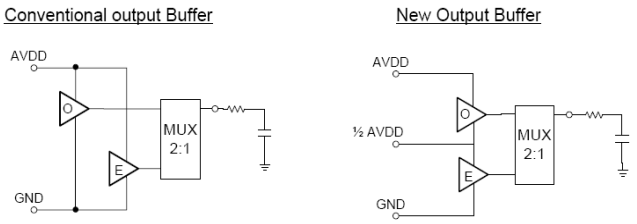

Fig. 3. Simplified source driver using AVDD/2 and AVDD supply

Figure 3 shows the simplified output buffer of the LCD source driver. The R-C network connected to the MUX represents the LCD pixel. The conventional solution is shown on the left and the new solution using AVDD and half of the source driver voltage,

AVDD/2. The new solution reduces the power dissipation in the source driver IC and the overall input current of the system. This requires an additional supply rail, typically half of the source driver voltage AVDD. The most appropriate solution to generate AVDD/2 depends mainly on the required load current. The required load current can be predicted by a detailed understanding of the source driver methodology, when driving each LCD pixel. By closer investigation it can be seen that the load current on AVDD/2 depends on the LCD inversion method and image content. In an ideal case the load current at AVDD/2 is close to zero. Special image pattern cause a much higher current on AVDD/2. In addition to that this supply rail has to sink and source current.
To implement such a solution 3 possible topologies can be used. The most common discrete solution uses a synchronous controller with external MOSFETS.

Possible solutions generating AVDD/2 supply

1. Operational Amplifier
2. Synchronous buck controller (external MOSFETs)
3. Synchronous integrated buck converter (integrated MOSFETs)

With all this background information it becomes clear that the best solutions in terms of cost, solution size and reliability is a fully integrated synchronous buck converter. An operational amplifier could get damaged because of excessive heat during specific image patterns and contents. The synchronous buck controller can be adjusted to the desired load current and power dissipation. Drawback is a larger solution size, more external components and total higher solution cost.
The AVDD/2 supply rail implementation just shows one example demonstrating the importance of *in detail system understanding*. While most discrete solutions use a synchronous controller the integrated solution uses an optimized synchronous step down converter.

3. Summary

Today's solutions already have a fairly high integration level enabling a complete solution using just a few ICs. Eventually only the timing controller, memory IC, LCD bias IC and maybe gamma buffer IC is required to complete the solution. Further maturation of the LCD application and technology improvements will lead to a solution that may require two ICs only. Ideally the ICs are simple to use, reliable and require a minimum of design in time and design expertise. The LCD system is a fairly complex system with interaction between LCD, control and supply circuits. The LCD bias IC development and implementation is therefore faster and simpler and more reliable with an experienced partner.

4. References

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