High gain pentacene inverter using different pentacene-thickness in several dielectrics

Sung-jin Mun[1], Kimoon Lee[1], Kwang-H. Lee[1], Min suk Oh[2] and Seongil Im[1]
[1]**Institute of Physics and Applied Physics, Yonsei University, Seoul 120-749, Korea**
Tel.:82-2-2123-2842, E-mail: semicon@yonsei.ac.kr
[2]**Korea Electronics Technology Institute (KETI), Seongnam 463-816, Republic of Korea**

Keywords: pentacene, inverter, dielectric, hysteresis

Abstract

The authors report on the fabrication of p-type depletion mode inverter that composed of two pentacene based thin-film transistors (TFTs) on several dielectric surfaces. We use shift of threshold voltage depends on pentacene-thickness.

1. Introduction

Pentacene inverter has been studied and fabricated with several methodologies as a fundamental element of conventional integrated circuit on glass or plastic.

Among the methodologies, using different W/L ratios for the load- and driver-TFTs, changing the dielectric surface of load- or driver-TFTs, adopting different polymer dielectrics for load and driver, using dual-gate for the driver-TFTs have been reported for pentacene inverter, all of which were based on the effort to change threshold voltage (V_{TH}) of load- or driver-TFTs.

In the present study, we adopt another but more simple way to change the V_{TH} of load-TFTs and achieve an organic inverter: changing the channel thickness.

2. Experimental

We used indium-tin-oxide (ITO)/glass that was cleaned with acetone, methanol, and de-ionized water, in that order. ITO gate electrodes were patterned by wet etching.

Then we deposited three kinds of dielectrics: sputter-deposited AlO_x, optimally-cured poly-4-vinyphenol (PVP).

Pentacene (Aldrich Chem. Co., 99% purity, no other distillation) active channel layers were patterned on the dielectric layers through a shadow mask by thermal evaporation at room temperature (RT). We fixed the pentacene deposition rate to 1 Å/s.

For source/drain (S/D) of the pentacene TFTs and also for inverter connection, Au was evaporated onto the pentacene channels at RT. Nominal channel length (L) and width (W) of our pentacene TFTs were 90 and 500 μm, respectively.

We used two different pentacene thicknesses for load- and driver-TFTs: 25 and 50 nm for OTFT inverter with dielectric AlO_x, but vice versa for other devices with PVP dielectric.

3. Results and discussion

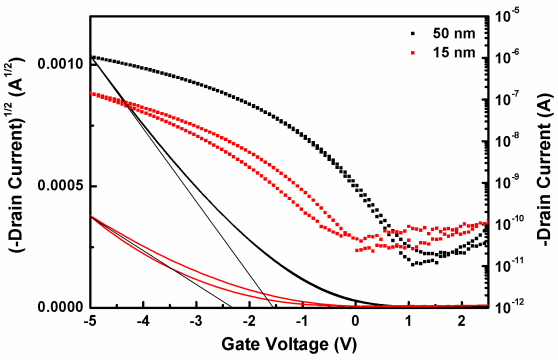

Fig. 1. $\sqrt{-I_D} - V_G$ and $\log_{10}(-I_D)$-V_G plots obtained from our pentacene TFTs with AlO_x dielectric at V_D = -8 V.

Fig. 1. shows the I_D versus gate voltage (V_G)

transfer curves of two pentacene TFTs with 100 nm-thick AlO_x dielectric that was deposited by 50 watt rf sputtering of Al_2O_3 target (~99.999%) at RT. Both OTFTs with 25 and 50 nm-thick channel appear very stable with little hysteresis, but one with 25 nm-thin channel displays smaller V_{TH} and higher on-state current. Since we previously observed the similar results from pentacene TFTs on hydrophilic SiO_2 dielectric where I_D and mobility gradually decreased with pentacene thickness due to thickness-induced resistance which is the parasitic resistance through thickness between the metal/pentacene interface and the channel, we set up a TFT inverter utilizing the thickness effects on hydrophilic AlO_x; 25 nm-thin pentacene channel was used for load-TFT while 50 nm-thick channel for driver-TFT.

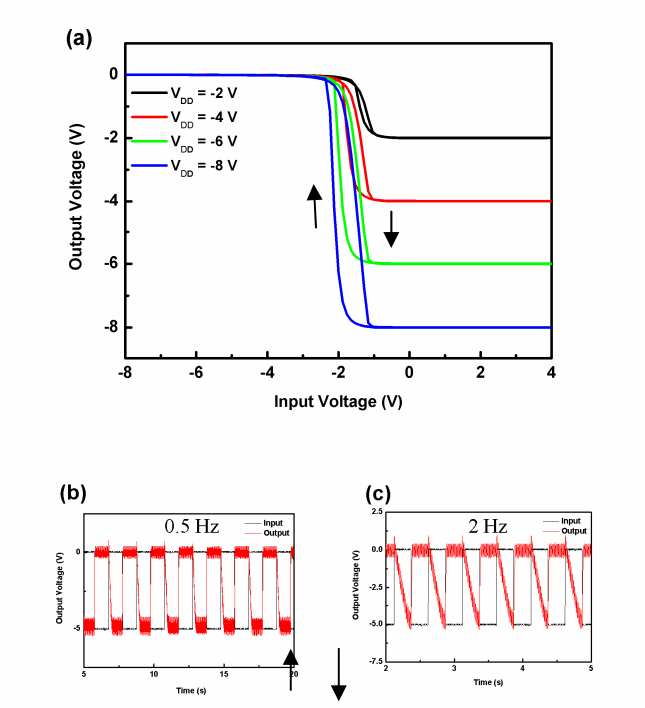

Fig. 2. (a) VTC of the inverter on AlO_x as obtained in different V_{IN} sweep range. Dynamic action of our inverter at (b) 0.5 Hz and (c) 2 Hz.

Fig. 2. (a) shows voltage transfer curves (VTCs). VTCs show some hysteresis at output voltage (V_{OUT}) switching, and all the hysteresis appears almost the same regardless of V_{IN} range when the sweep started from negative voltages to reach the positive values. During V_{IN} sweep, electron injection from ITO gate electrode into AlO_x or time-dependent charge trapping at the pentacene/dielectric interfaces are expected and such mobile charge behavior causes the visible hysteresis in the driver TFT side. If our pentacene TFT driver of this inverter was influenced by time-dependent charge trapping at the pentacene/dielectric interfaces, the hysteresis direction would appear opposite to the present direction. Therefore, the observed VTC hysteresis is attributed to the electron injection from the ITO gate.

Fig. 2. (b) and (c), the dynamic actions of our inverter are demonstrated. At a low frequency, the inverting action was clearly observed along with the discharging- and charging-induced signal peaks (or RC-delays at in and off switching). This RC time delay was unavoidable because of a large overlap capacitance between V_{IN} and V_{OUT} probes in our simple inverter structure.

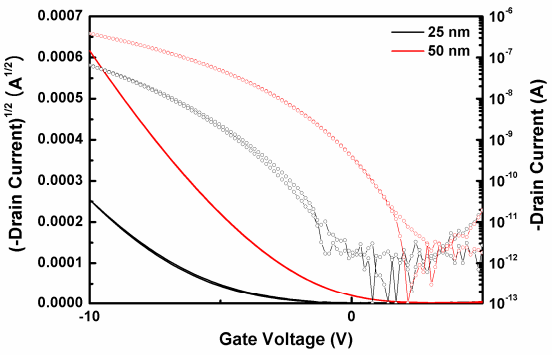

Fig. 3.$\sqrt{-I_D}$ – V_G and $\log_{10}(-I_D)$-V_G plots obtained from our pentacene TFTs with AlO_x dielectric at V_D = -10 V.

We also tested the case of PVP polymer for an inverter dielectric, on which OTFT with 25 nm-thin pentacene channel has lower on-state I_D and larger V_{TH} than that with 50 nm-thick channel. The transfer curves of Fig. 3. shows the very results, supporting previous reports that a hydrophobic dielectric surface has an optimum pentacene channel thickness around 50 nm. Unlike the case on hydrophilic oxide of large surface energy, the pentacene channel on hydrophobic dielectric doesn't have perfect coverage if it is too thin, so that the channel conductance of 25 nm-thin pentacene may be smaller than that of 50 nm-thick channel. In this case, we set up an inverter taking 50 nm-thick pentacene as the channel of load-TFT because this TFT with 50 nm-thick channel has lower V_{TH} (-3.6 V) than that (-6 V) with 25 nm-thin

pentacene channel, which is now contrary to the case on hydrophilic AlO_x.

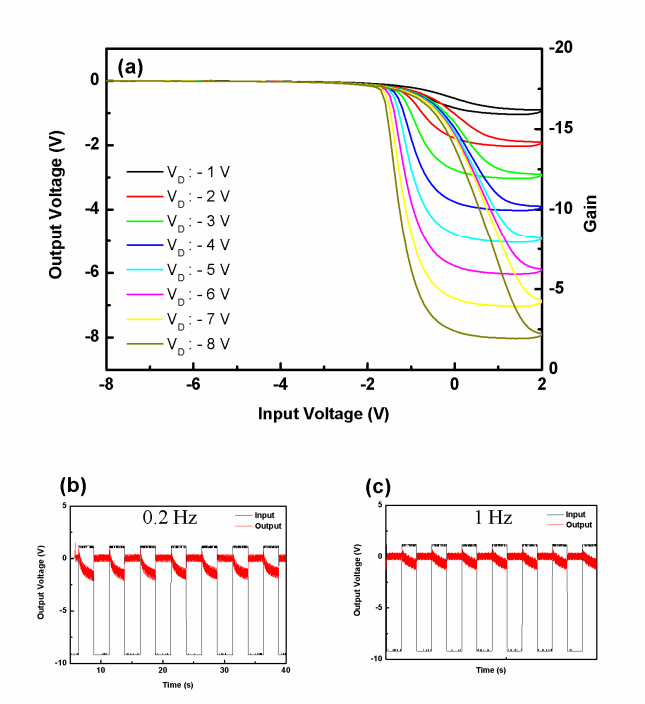

Fig. 4. (a) VTC of the D-inverter on PVP as obtained in different V_{IN} sweep range. Dynamic action of our inverter at (b) 0.2 Hz and (c) 1 Hz.

Fig. 4. (a) shows VTCs of depletion-mode inverter (D-inverter). Although OTFTs with this polymer dielectric did not show any gate-bias hysteresis in their transfer curves, our D-inverter VTCs behavior displayed very large hysteresis depending on V_{IN} sweep range. The stress would easily cause gate electron injection into the thick PVP as well as cause electric dipoles in PVP. The dipoles in PVP are slowly depolarized even at a positive (+) V_{IN} during the sweep. Fig. 4. (b) and (c) show the dynamic actions of our inverter.

We also fabricated enhance-mode inverter (E-inverter). Fig. 5. (a) shows VTCs of E-inverter. Although our E-inverter shows low gain, dynamic action is showed better result than D-inverter. Fig. 5. (b), (c), (d) and (e) show the dynamic actions of our inverter.

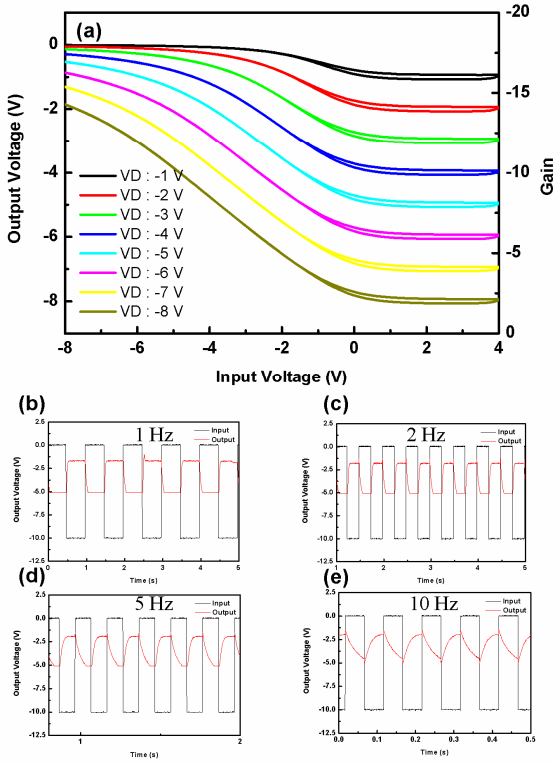

Fig. 5. (a) VTC of the D-inverter on PVP as obtained in different V_{IN} sweep range. Dynamic action of our inverter at (b) 1 Hz and (c) 2 Hz (b) 5 Hz and (c) 10 Hz.

4. Summary

We have fabricated p-channel depletion and enhanced mode inverter using two pentacene TFTs with different channel thicknesses. Our inverter on PVP dielectric shows very large hysteresis depending on V_{IN} sweep range due to dipole in polymer. And inverter on AlO_X dielectric shows a little hysteresis due to charge injection.

Acknowledgement

The authors acknowledge the financial support from KOSEF (NRL program: grant No. 2009-8-0403), from the MKE [IT R&D program (2006-S079-02), Information Display R&D center, one of the 21st Century Frontier R&D Program, and fundamental R&D Program for Core Technology of Materials] and

from Brain Korea 21 program.

5. References

1. M. S. Oh, K. Lee, K. H. Lee, S. H. Cha, J.-M. Choi, B. H. Lee, M. M. Sung, and S. Im, Adv. Funct. Mater, **19**, 726 (2009).
2. J.-M. Choi, J. H. Kim, and S. Im, Appl. Phys. Lett, **91**, 083504 (2007).
3. S. Mun, J.-M. Choi, K. H. Lee, K. Lee and S. Im, Appl. Phys. Lett, **93**, 233301 (2008).
4. J. B. Koo, S. J. Yun, J. W. Lim, S. H. Kim, C. H. Ku, S. C. Lim, J. H. Lee, and T. Zyung, Appl. Phys. Lett, **89**, 033511 (2006).
5. J. Lee, K. Kim, J. H. Kim, D. -Y. Jung, and S. Im, Appl. Phys. Lett, **82**, 4169 (2003).
6. D. K. Hwang, M. S. Oh, J. M. Hwang, J. H. Kim and S. Im, Appl. Phys. Lett, **92**, 013304 (2008).