# Protective Layer on Active Layer of Al-Zn-Sn-O Thin Film Transistors for Transparent AMOLED

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## Abstract

*We have studied transparent top gate Al-Zn-Sn-O (AZTO) TFTs with an $Al_2O_3$ protective layer (PL) on an active layer. We also fabricated a transparent 2.5 inch QCIF+ AMOLED display panel using the AZTO TFT back-plane. The AZTO active layers were deposited by RF magnetron sputtering at room temperature and the PL was deposited by ALD with two different processes. The mobility and sub-threshold slope were superior in the cases of the vacuum annealing and the oxygen plasma PL compared to the $O_2$ annealing and the water vapor PL, however, the bias stability was excellent for the TFTs of the $O_2$ annealing and the water vapor PL.*

## 1. Introduction

Amorphous oxide thin film transistors have been intensively investigated for active matrix organic light emitting diode (AMOLED) displays recently. The reliable TFT array showing good electrical performance is indispensable for the large-size displays which are commercially available. Conventional a-Si TFT can be fabricated with high uniformity and low cost, however its mobility and bias stability are poor.[1] LTPS (low temperature poly silicon) TFT has disadvantages for large size production due to relatively poor uniformity and high cost.[2] Amorphous oxide TFT has relatively high mobility, good uniformity, good stability, and low cost processing. For these reasons, oxide TFTs such as ZnO[3], In-Zn-O[4], Zn-Sn-O[5] and IGZO[6] TFT have been widely studied. We have reported the oxide TFTs with a novel active layer which was composed with $Al_2O_3$-ZnO-$SnO_2$ (AZTO) and sputtered at room temperature.[7] The AZTO material is very stable chemically, and sputtering method has advantages on low cost and large area uniformity among various deposition methods. Therefore, the AZTO TFT is prominent device for driving the large size AMOLED panel. The active-insulator interface is known to be very important to control the electrical characteristics and stability of TFTs. In this study, we report the AZTO TFT characteristics depending on protective layers on active layers with top gate structure.

## 2. Experimental

We have fabricated the top gate TFTs with the active layer composed with $Al_2O_3$-ZnO-$SnO_2$ (AZTO). The schematic diagram of the top gate AZTO TFT structure is shown in Fig. 1. A 100x100 $mm^2$ alkaline-free glass was used as a substrate after the ultrasonic cleaning with acetone, iso-propyl alcohol and DI water in sequence. Gate and source/drain electrodes were constituted with 150 nm-thick ITO (indium tin oxide). A gate insulator of $Al_2O_3$ was formed by atomic layer deposition (ALD) method at 150 $^oC$ and its thickness was 180 nm. An AZTO layer was formed by co-sputtering of an $Al_2O_3$-ZnO target and a $SnO_2$ target with an off-axis type RF magnetron sputter at room temperature. The sputtering was performed in the atmosphere of Ar and $O_2$ mixed gas with the chamber pressure of 0.2 Pa. The protective layers were 9 nm-thick $Al_2O_3$ deposited by ALD method using tri-methyl aluminum (TMA) and water vapor or TMA and oxygen plasma. All patterning processes were performed by photo-lithographic method and wet etching process. The annealing was performed at 300$^oC$ in vacuum or $O_2$ atmosphere using electric ovens. The electrical characteristics of the TFTs were measured with the semiconductor parameter analyzer (Agilent B1500A). The bias stabilities of the TFTs were measured with other semiconductor analyzer (HP 4145B). The protective layer (PL) was deposited on active layer before active patterning, therefore, the interface between active layer and gate insulator was not attacked by chemical reactants which are used in

photolithography and etching processes. The interface between the PL and active layer is most important for TFT channel characteristics. We have prepared two types of PL, one is deposited at 200 °C with water vapor as an oxygen precursor and the other is deposited at 200 °C with oxygen plasma as an oxygen precursor. In each case, tri-methyl aluminum (TMA) was commonly used as an Al precursor. The active layers were deposited in the same condition of sputtering chamber, but annealed in two different atmosphere (oxygen atmosphere and vacuum) at 300 °C before PL deposition.

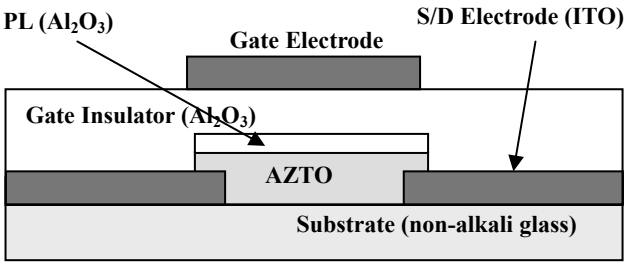



Fig. 1 Schematic diagram of the top gate AZTO TFT.

## 3. Results and discussion

The transfer characteristics of the AZTO TFTs prepared with different processes are shown in upper side of Fig. 2 - 5 and the transfer curve shifts of the TFTs under +20 V gate bias stress are shown in lower side of Fig. 2 - 5. The AZTO TFT annealed in $O_2$ and including the water vapor PL showed a field effect mobility ($\mu_{FET}$) of 12.9 $cm^2$/Vs, a sub-threshold slope (S/S) 0.28 V/dec, and a turn-on voltage (Von) -0.8 V. The AZTO TFT annealed in $O_2$ and including oxygen plasma PL showed the $\mu_{FET}$ 15.2 $cm^2$/Vs, the S/S 0.14 V/dec, and the Von -0.8 V. The AZTO TFTs annealed in vacuum and including water vapor PL, and annealed in vacuum and including oxygen plasma PL showed the $\mu_{FET}$ 14.4 $cm^2$/Vs and 16.6 $cm^2$/Vs, the S/S 1.0 V/dec and the 0.15 V/dec, and the Von -8.5 V and -0.2 V, respectively. The mobility and the sub-threshold slope of the AZTO TFTs including the oxygen plasma PL were superior compared to those of the water vapor PL TFTs. On the other hand, the Von shifts under +20 V gate bias for 167 minutes of the AZTO TFTs annealed in $O_2$ and including the water vapor PL, and annealed in $O_2$ and the oxygen plasma PL were 0.7 V and 5.8 V, respectively. The Von shifts of the TFTs annealed in vacuum and including the water vapor PL, and annealed in vacuum and

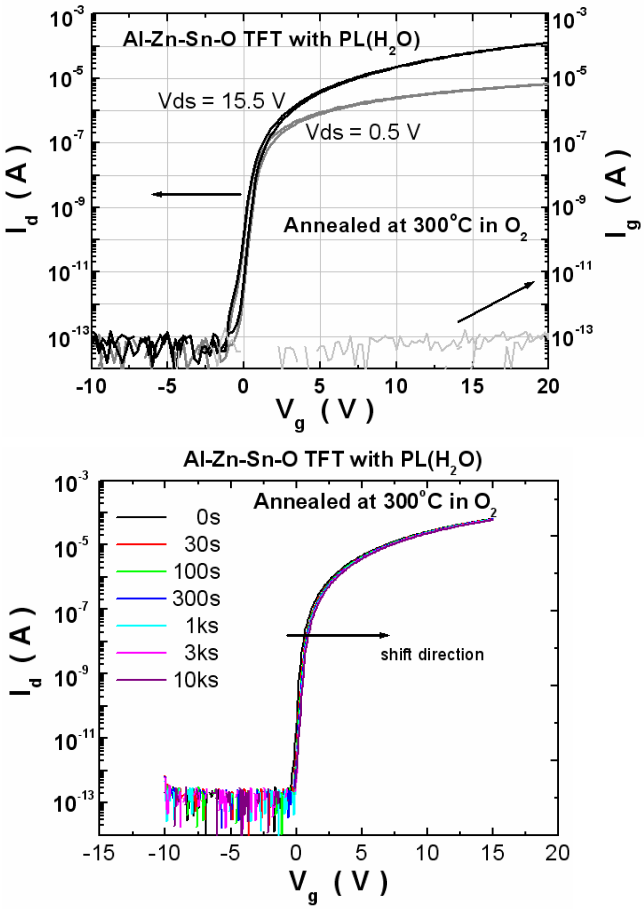



Fig. 2 Transfer characteristics (upper) and transfer curve shift (lower) of the AZTO TFT annealed in O2 and including water vapor PL.

including oxygen plasma PL were 0.8 V and 8.9 V, respectively. The bias stability was excellent in the TFTs of the water vapor PL. The bias stability of the TFTs including the oxygen plasma PL was relatively poor compared to that of the water vapor PL. The mobility and the sub-threshold slope were good in the cases of the vacuum annealing and the oxygen plasma PL compared to the $O_2$ annealing and the water vapor PL, however the bias stability was good in the case of the $O_2$ annealing and the water vapor PL compared to the vacuum annealing and the oxygen plasma PL. The sub-threshold slope is known to increase with increasing active-insulator interface traps,[8] thus the vacuum annealing and oxygen plasma PL are considered to reduce the interface traps. The turn-on voltage was shifted to positive side with positive gate bias as shown in Fig. 2 - 5. The charge trapping at the active-insulator interface is supposed to be the main

origin of the bias instability. Therefore, the activation energy that carriers pass over the interface and trap in the insulator is thought to be high in the case of $O_2$ annealing and water vapor PL.[9] As a result of this

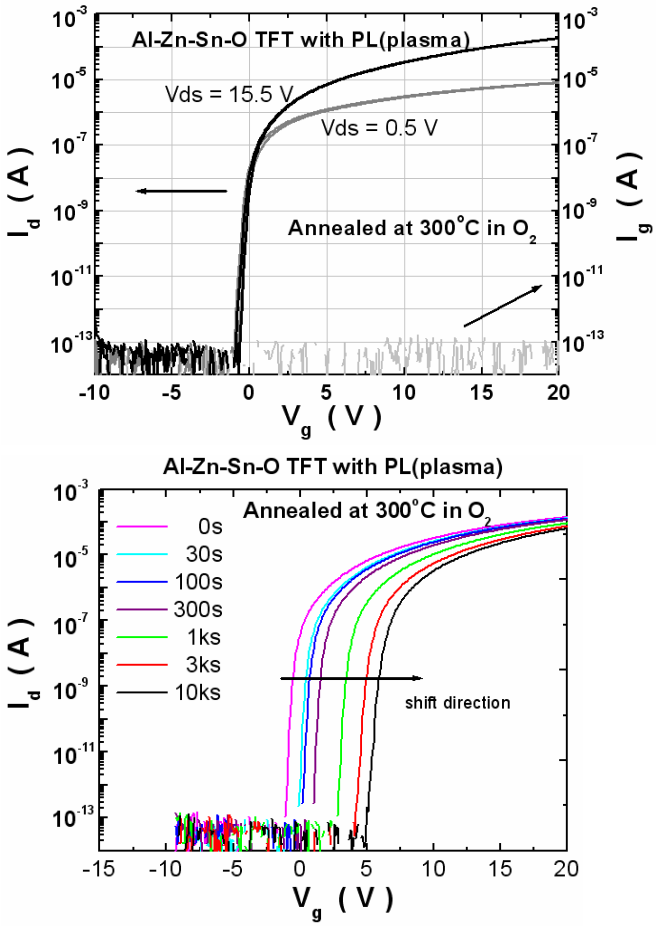



Fig. 3 Transfer characteristics (upper) and transfer curve shift (lower) of the AZTO TFT annealed in O2 and including oxygen plasma PL.

origin of the bias instability. Therefore, the activation energy that carriers pass over the interface and trap in the insulator is thought to be high in the case of $O_2$ annealing and water vapor PL.[9] As a result of this study, the $O_2$ annealing and water vapor PL increase the number of the active-insulator interface traps, however they make the charge trapping at the interface and insulator difficult. The charge trapping site and mechanism causing the bias instability are suppose to be different from those causing the sub-threshold slope degradation for the AZTO TFTs.

We have successfully manufactured the 2.5 inch AMOLED panel using the back-plane with the stable

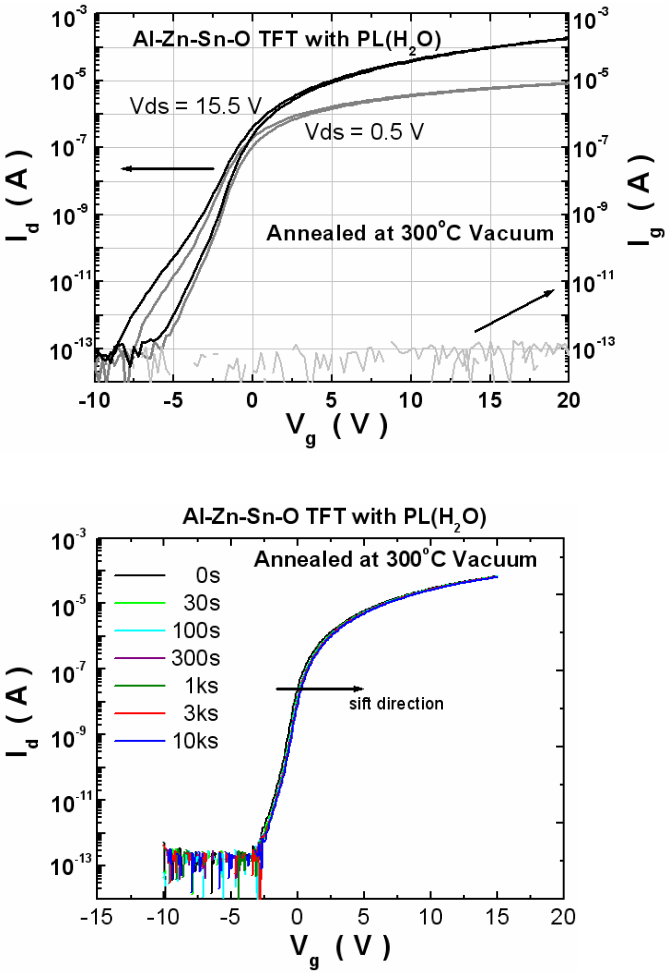
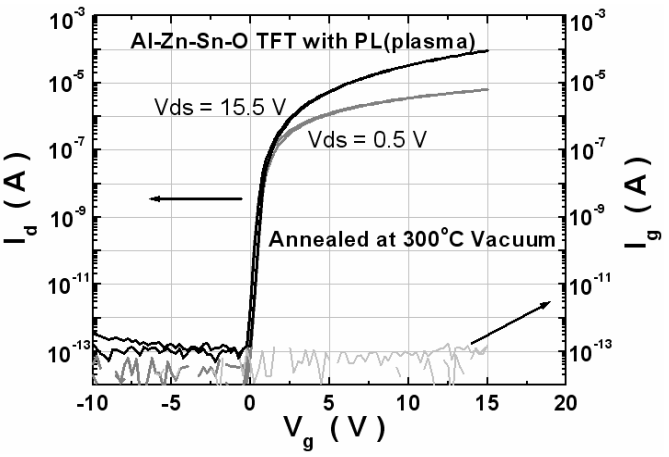



Fig. 4 Transfer characteristics (left) and transfer curve shift (right) of the AZTO TFT annealed in vacuum and including water vapor PL.



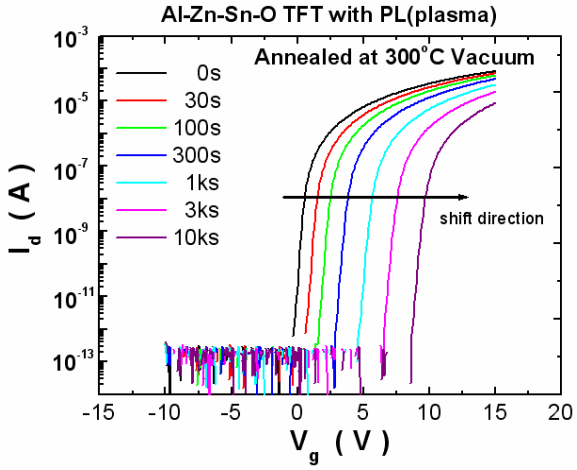



Fig. 5 Transfer characteristics (left) and transfer curve shift (right) of the AZTO TFT annealed in vacuum and including oxygen plasma PL.

top gate AZTO TFT including the water vapor PL as shown in Fig. 6. The AMOLED specification was QCIF+; 176 X 220, and monochrome.

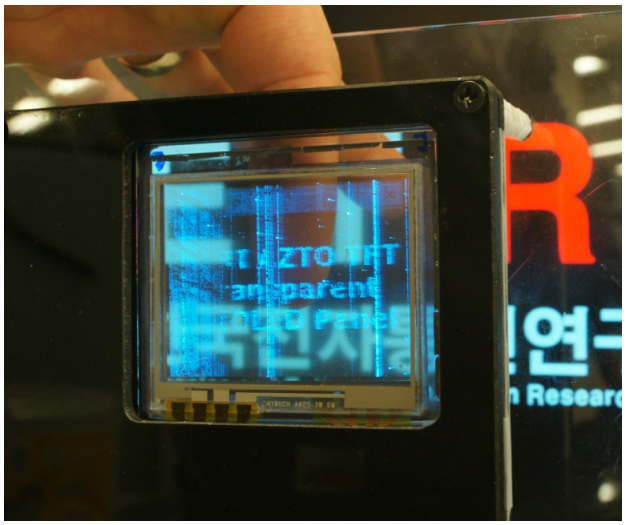


Fig. 6 AMOLED panel using the top gate AZTO TFT back-plane.

## 4. Summary

We have manufactured stable AZTO TFTs with active layer which was deposited at room temperature and processed at low temperature. We also investigated the origins of TFT characteristic change and the bias instability by using the different PL and active annealing process. The active-insulator interface control in the oxide TFT manufacturing process is very important for the improvement of the TFT characteristics and stability. The AZTO layer was deposited by sputtering which is convenient for large size commercial production. The film deposition at room temperature and the low temperature processing is significant advantages for the fabrication of flexible electronics. The AZTO TFT is considered to be an excellent candidate for application to large size flexible displays and electronics with plastic substrates. We are developing the optimum conditions of the AZTO TFT fabrication process for better performance, and the electrical characteristics of the AZTO TFT will be improved. We have also manufactured the transparent 2.5 inch AMOLED panel driven by AZTO TFT back-plane prepared by low temperature process.

## 5. References

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