

A Novel Two-Switch Active Clamp Forward Converter for High Input Voltage Applications

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Abstract

A novel two-switch active clamp forward converter suitable for high input voltage applications is proposed. The main advantage of the proposed converter, compared to the conventional active forward converters, is that circuit complexity is reduced and the voltage stress of the main switches is effectively clamped to either the input voltage or the clamping capacitor voltage by two clamping diodes without limiting the maximum duty ratio. Also, the clamping circuit does not include additional active switches, so a low cost can be achieved without degrading the efficiency. Therefore, the proposed converter can feature high efficiency and low cost for high input voltage applications. The operational principles, features, and design considerations of the proposed converter are presented in this paper. The validity of this study is confirmed by the experimental results from a prototype with 200W, 375V input, and 12V output.

1. Introduction

Most of the PC power supply system has two stages as shown in Fig.1. It is customary to add a front-end rectifier part, which functions as the power-factor correction for the standards of the harmonic regulation. The nominal voltage of 400V obtained from ac-line voltage (90-265 V_{rms}) should be converted to the lower voltages such as 12V, 5V, and 3.3V for HDD, graphic card, on-board DC/DC converter and so on. The DC/DC converter performs this conversion and requires low output voltage, high output current, and high efficiency. The forward converter topology is one of the most popular switching topologies for low and medium power applications. In particular, the forward with the active-clamp reset offers many advantages over the forward converter with other reset methods: the active reset circuit, switching operation with duty-cycle higher than 50%, and achievement of zero-voltage switching (ZVS) [1]-[3]. However, it is not suitable for high input voltage applications. The power factor correction (PFC) circuit using a boost rectifier of which output voltage is around 400Vdc. In this case, the voltage stresses on switches are greater than 800V. Thus, high voltage rating switches should be used and in consequence efficiency and cost are degraded.

In the circuit [3], only two small clamping diodes are used for reducing the voltage stress and eliminating the imbalance problem of the two main switches. Both of the main switches are clamped to the input voltage. Also, compared to the previous converters, the cost can be reduced considerably. However, since the clamp capacitor is also clamped to the input voltage, the maximum duty ratio is limited to under 50%. For wide range input voltage applications such as the applications with the hold-up time requirement, this converter is not appropriate.

This paper proposes a novel two-switch active clamp forward (ACF) converter with two clamping diodes. The ZVS mechanism of the main and auxiliary switch is the same as that of the conventional ACF converters. The two clamping diodes provide not only clamping the voltage of the main switches, but

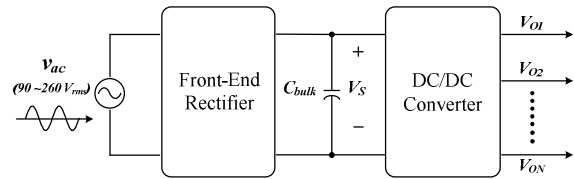


Figure 1. Typical PC power supply

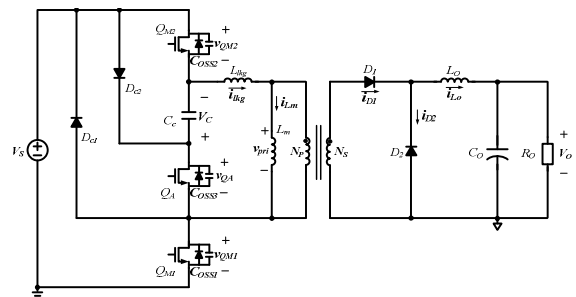


Figure 2. Proposed two-switch active clamp forward converter

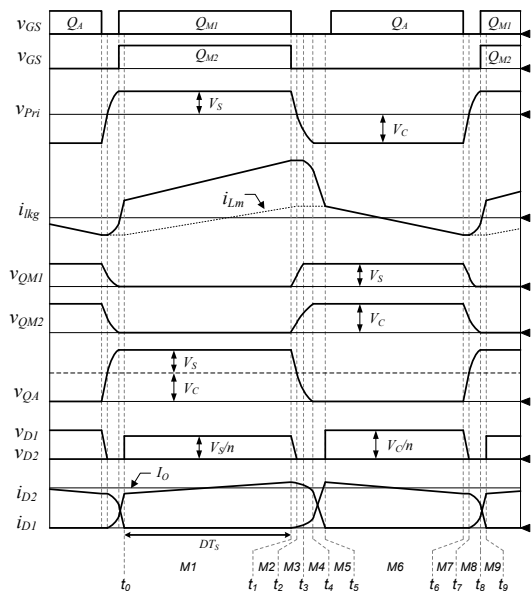


Figure 3. Key waveforms for the mode analysis.

also increasing the duty ratio to over 50% without additional components, compared to the converter [3].

2. Operational Principle

Fig. 2 shows the circuit configuration of the proposed two-switch ACF converter. The main switches Q_{M1} and Q_{M2} are operated in a duty ratio of D , and the switch Q_A is operated with complementary to the main switches. Fig. 3 shows the key

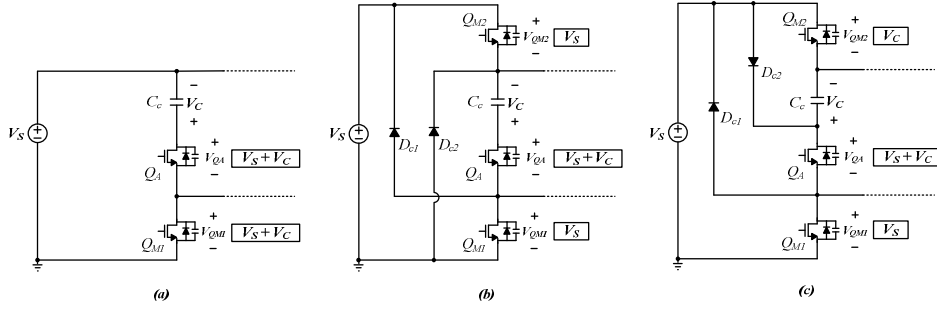


Figure 4. Comparison of the switch voltage stress of the primary circuits (a) conventional ACF converter, (b) ACF converter [3], and (c) proposed converter

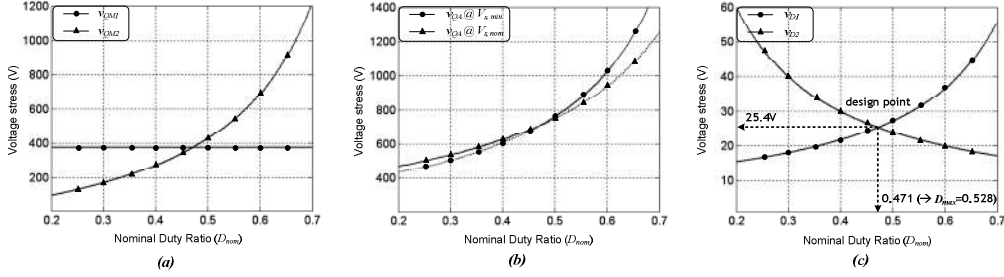


Figure 5. The voltage stress of the switches and diodes, assuming $P_O=200$ -W, $\eta=88\%$, and $C_{bulk}=270$ -uF. (a) main switches (Q_{M1} and Q_{M2}), (b) auxiliary switch (Q_A), and (c) secondary diodes (D_1 and D_2)

operating waveforms of the proposed converter in the steady state.

Mode 1 [$t_0 \sim t_1$]: Mode 1 begins when the commutation of $i_{D1}(t)$ and $i_{D2}(t)$ is completed. Then, $i_{Lo}(t)$ flows through D_1 . Since Q_{M1} and Q_{M2} are on state and Q_A is off state, V_S is applied to $L_{lk} + L_m$ and $V_S/n - V_O$ is applied to L_O where $n=N_p/N_s$ is transformer turns ratio. Therefore, the power is transferred from input source to output.

Mode 2 [$t_1 \sim t_2$]: This mode begins when Q_{M1} and Q_{M2} are turned off. Until $v_{pri}(t)$ becomes 0 V, diode D_2 is still reverse biased. It assumes that $i_{lk}(t_1)$ is constant during this mode. Therefore, C_{OSS1} , C_{OSS2} , and C_{OSS3} are linearly charged and discharged by $i_{lk}(t)$, respectively.

Mode 3 [$t_2 \sim t_3$]: When $v_{QM1}(t) + v_{QM2}(t)$ increases to V_S , $v_{pri}(t)$ reaches 0V and $i_{Lo}(t)$ begins to freewheel through D_1 and D_2 . C_{OSS1} and C_{OSS2} are charged and C_{OSS3} is discharged in a resonant manner of L_{lk} and $3/2C_{OSS}$. As $i_{lk}(t)$ decreases, $i_{D1}(t)$ decreases and $i_{D2}(t)$ increases.

Mode 4 [$t_3 \sim t_4$]: This mode begins when $v_{QM1}(t)$ is clamped to V_S through D_{C1} , and $i_{lk}(t)$ freewheels through D_{C1} . L_{lk} resonates with $C_{OSS2} + C_{OSS3} = 2C_{OSS}$.

Mode 5 [$t_4 \sim t_5$]: After v_{QM2} reaches V_C , D_{C2} turns on and clamps the Q_{M2} . $i_{lk}(t)$ flows through the body diode of Q_{M2} and the ZVS of Q_{M2} is achieved. Because D_1 and D_2 are conducting, the voltage across the transformer is 0V and V_C is all reversely applied to L_{lk} . Therefore, $i_{lk}(t)$ rapidly decreases.

Mode 6 [$t_5 \sim t_6$]: When $i_{lk}(t)$ reaches the transformer magnetizing current $i_{Lm}(t)$, D_1 is turned off with D_2 still conducting. Since V_C is applied to $L_m + L_{lk}$ and V_O is applied to L_O reversely.

Mode 7 [$t_6 \sim t_7$]: This mode begins when Q_A is turned off. $i_{lk}(t)$ charges C_{OSS3} and discharges C_{OSS1} and C_{OSS2} simultaneously. It is assumed that $i_{lk}(t_6)$ is constant during this mode. Thus, $v_{QA}(t)$ increases, and $v_{QM1}(t)$ and $v_{QM2}(t)$ decreases.

Mode 8 [$t_7 \sim t_8$]: After $v_{QM1}(t) + v_{QM2}(t)$ decreases to V_S , $v_{pri}(t)$ reaches 0V and $i_{Lo}(t)$ begins to freewheel through D_1 and D_2 . C_{OSS1} and C_{OSS2} are discharged and C_{OSS3} is charged in a resonant manner of L_{lk} and $3/2C_{OSS}$. As $i_{lk}(t)$ decreases, $i_{D1}(t)$ increases and $i_{D2}(t)$ decreases.

Mode 9 [$t_8 \sim t_9$]: After $v_{QM2}(t)$ reaches 0V, $i_{lk}(t)$ flows through the body diode of Q_{M2} and the ZVS of Q_{M2} is achieved. Because D_1 and D_2 are still conducting, the voltage across the transformer is 0V and V_S is all applied to L_{lk} . At t_9 , the commutation between $i_{D1}(t)$ and $i_{D2}(t)$ is finished.

3. Features and Characteristics

The DC conversion ratio of the proposed converter is the same as that of the conventional ACF converter as following equation (18).

$$\frac{V_O}{V_S} = D \times n. \quad (18)$$

A. Effective Clamping Circuits

The primary circuits and the voltage stresses of the switches of conventional two-switch ACF converters [3] and the proposed converter are compared in Fig. 4. The conventional ACF converter has only one main switch and no additional clamping circuit as shown in Fig. 4(a). The voltage stress of the main switch is $V_S + V_C$. Because the load current (I_O/n) flows through the main switch, the voltage rating of the main switch which influences the drain-source resistance of MOSFET is important. Therefore the efficiency of the conventional ACF converter with a main switch of high voltage rating would be degraded. The converter [3] has two main switches and two additional clamping diodes, as shown in Fig. 4(b). The two clamping diodes are used for clamping each main switch to the input voltage. Therefore, low voltage rating switches can be used and efficiency can be increased. However, the two clamping diodes also clamp the clamping capacitor C_C to the input voltage. Therefore, the maximum duty ratio is limited to 50%. The proposed ACF converter consists of two main switches and two clamping diodes, as shown in Fig. 4(c). Unlike the converter [3], Q_{M2} is clamped to C_C through D_{C2} . The clamping path of the clamping capacitor through two diodes can not be maintained and clamping capacitor voltage can vary over input voltage. Therefore, the maximum duty ratio can be increased to over 50%.

B. Device Voltage Stress

The voltage stress of each switch is given by

$$v_{QM1} = V_{S,nom}, \quad (19)$$

$$v_{QM2} = V_C = \frac{D_{max}}{1-D_{max}} \times V_{S,min}, \quad (20)$$

$$v_{QA} = V_S + V_C = \max \left[\frac{1}{1-D_{nom}} \times V_{S,nom}, \frac{1}{1-D_{max}} \times V_{S,min} \right] \quad (21)$$

where, $V_{S,nom}$ and D_{nom} is the nominal input voltage and nominal duty ratio, respectively and $V_{S,min}$ is the minimum input voltage which is reached after the hold-up time.

The voltage stress of Q_A has two different forms according to the duty ratio and the maximum value of the two is the stress of Q_A . It is assumed that the output voltage of the PFC circuit is well regulated at $V_{S,nom}$. Thus, $V_{S,nom}$ is the maximum voltage of the bulk capacitor.

The voltage stress of each diode is given by

$$v_{D1} = \frac{1}{1-D_{max}} \times V_O, \quad (22)$$

$$v_{D2} = \frac{1}{D_{nom}} \times V_O. \quad (23)$$

4. Design Considerations

A. Considering the Hold-Up Time

Hold-up time requirement is special requirement for PC power systems. It requires the system to provide output voltage within regulation for 17ms after loss of AC input at full load condition. Therefore, hold-up time should be considered to decide the nominal and maximum duty ratio.

B. Decision of the nominal duty ratio

Fig. 5 shows voltage stresses of each device according to nominal duty ratio D_{nom} . As seen in Fig. 5, the voltage stress of Q_{M1} is nominal input voltage and that of Q_{M2} increases according to the duty ratio as shown in Fig. 5(a). The voltage stress of Q_A can be obtained in two cases of $V_{S,min}$ and $V_{S,nom}$. As shown in Fig. 6(b), the bold line is the maximum voltage stress of Q_A . The voltage stress of D_2 increases and that of D_1 decreases according to the duty ratio as shown in Fig. 5(c). However, the nominal duty ratio for minimum voltage stress of the two secondary diodes can be accomplished at the node (design point) in Fig. 5(c).

5. Experimental Results

A 200W prototype of the proposed two-switch ACF converter with 375V input and 12V output operating at 72kHz has been built and tested to verify the principles of operation. The nominal duty ratio is 47.1% and the maximum duty ratio of 52.8% is used to minimize the voltage stresses of the secondary diodes. The minimum input voltage is about 335V.

Fig. 6 shows the waveforms of the primary voltage, leakage current, switches voltage and the secondary diode voltages at nominal input voltage and full load. Fig. 7 shows the measured efficiencies of the proposed two-switch ACF converter with the conventional ACF converter for comparison. The maximum overall efficiency is about 88%.

6. Conclusion

A novel two-switch ACF converter using the clamping diodes is presented. The proposed converter has features such as low voltage stress of main switches, low cost, wide range of duty ratio and high efficiency. Through the experiment, it is confirmed that the voltage stresses of the main switches are effectively clamped to either the input voltage or the clamping

capacitor voltage. Moreover, the experimental result shows that the efficiency of the proposed converter is higher than that of the conventional ACF converter at all load conditions. Therefore, the proposed converter is well suited for high input voltage applications.

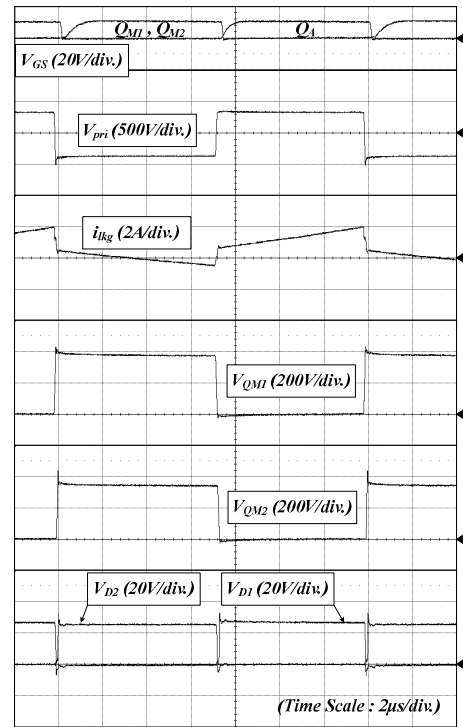


Figure 6. Key experimental waveforms at 375-V, full-load condition.

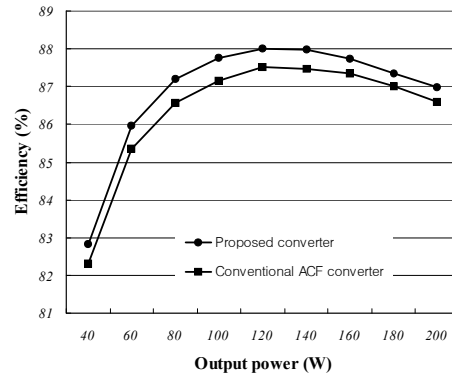


Figure 7. Efficiency comparison under the load variation

Acknowledgment

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