A New Four Level Half-bridge Converter

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Abstract

A new four level half-bridge converter is proposed in this paper. Compared to a conventional half-bridge converter and an asymmetric half-bridge converter, the proposed converter has less stress on power switching components and have smaller output inductor. Zero-voltage-switching condition is also achieved with the proposed converter. The operational principle, DC conversion ratio and ZVS analysis are presented. Experimental results are demonstrated to verify the feasibility and advantages of the new topologies.

1. Introduction

As function of computer and telecommunication devices are advanced, requirements for converters used in server power, PC power and telecommunication are getting more complicated. To meet these rigorous requirements (such as zero-voltage switching, high power density, high efficiency and low EMI property) various control techniques and many new topologies have been suggested. In half-bridge topologies, widely used in medium power application, an asymmetric duty cycle control technique has been recognized as a candidate for high-density and high-efficiency dc/dc power converter applications due to its zero-voltage-switching (ZVS) condition. However, in general, it also suffer from these limitations: 1) Duty cycle is limit under to $0<D<0.5$ and it is far more restricted under wide input voltage range; 2) Voltage stress on the output rectifier is unbalanced due to asymmetric switching time of the main switches; 3) DC offset current is showed, it reduce the utilization of the transformer and it leads to increase the current rating of the main switches. Some of these limitations can be overcome by adopting two-transformer to enlarge the duty cycle[2] or adopting one more switch on the rectifier side[3]. However, in these cases, transformer should be doubled or control technique becomes difficult.

In the proposed converter, voltage stress on the output rectifier is equally distributed and it has no dc offset current. It also achieve good zero-voltage-switching condition in all switches and output inductor size can be reduced. The operational principles, analysis and experimental results are presented to confirm the validity of the proposed converter.

2. Operation Principle

2.1 Circuit configuration

Fig.1 shows the circuit diagram of the proposed converter and Fig.2 is its key waveforms in steady state. A small transformer and small two switches are connected to the conventional half-bridge circuit. Compare to an asymmetric half-bridge converter, the proposed converter needs one more transformer and two more switches in the primary side. However, when considering the size and efficiency, the proposed converter shows better performance.

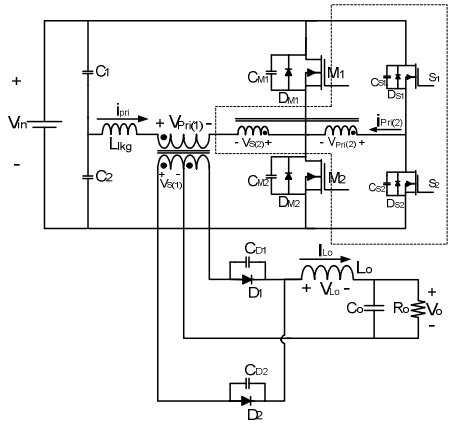

Fig. 1 A New Four Level Half Bridge Converter

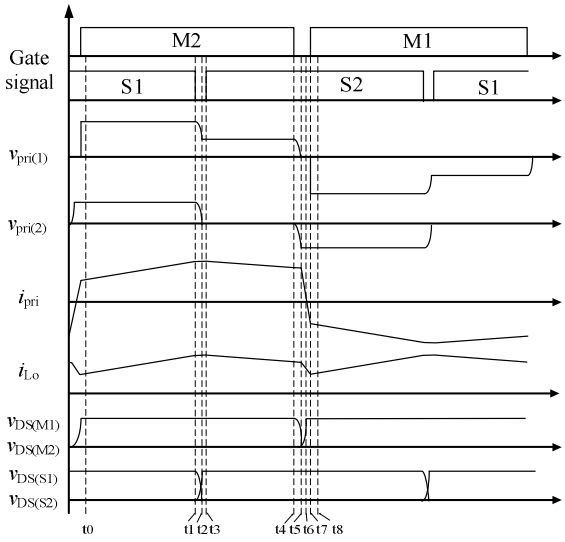

Fig. 2 Key Waveforms of the Proposed Converter

The transformer size can be reduced compare to an asymmetric half-bridge converter because it has no DC offset current with its symmetric switching control and the size of the added components is smaller than the main components. Also the output filter inductor size is reduced because the frequency shown at output filter of the proposed converter is twice faster than the one in an asymmetric half-bridge converter.

2.2 Operation Principle

For the convenient analysis of the steady state operation several assumptions are made as follows;

a) All parasitic components except for the leakage inductor are neglected,

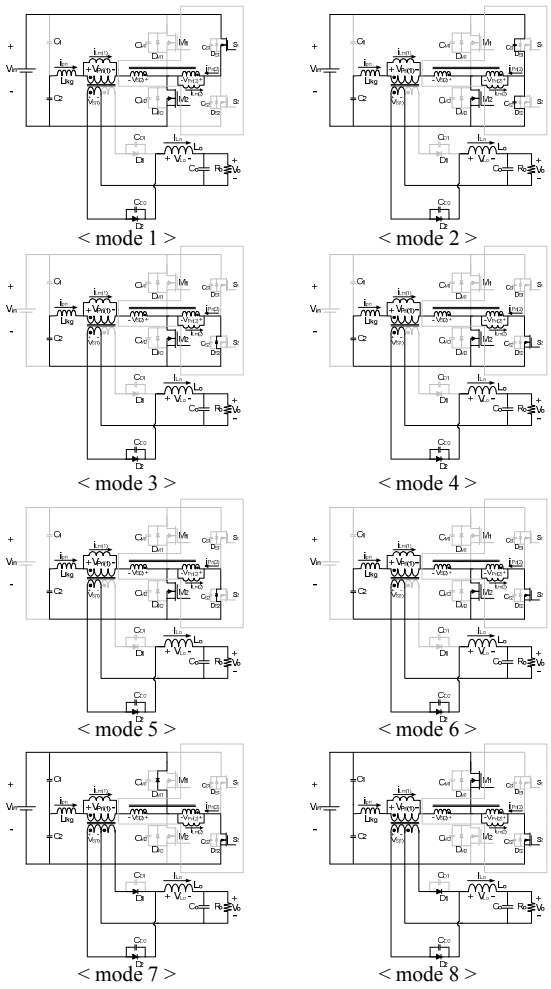

Fig. 3 Equivalent circuit of the proposed converter

b) The switches M1, M2, S1 and S2 are ideal except for their output capacitors and body diodes,
c) The capacitors, C1 and C2, are large enough to be considered as a constant voltage source (1/2)Vs,
d) Turn ratio of the main transformer is n1=N1/N2 and n2=Ns1/Ns2 for the sub transformer.
e) The primary current is constant during the very short period; t_1~t_2, t_2~t_3 and t_4~t_5

Mode 1(t_0~t_1) : Mode 1 begins when the commutation of the secondary rectifier diode is completed. Input energy is transferred into the secondary side in this mode by main-switch M2, sub-switch S1 and transformers. At this time, the larger voltage is applied to the main transformer than the voltage in asymmetric half-bridge converter so it helps to reduce the conduction loss in primary side. The transformer voltage and primary/secondary current are given as:

$$V_{pri(2)} = V_s, \qquad V_{pri(1)} = \frac{1}{2}V_s + \frac{1}{n_2}V_{pri(2)} \tag{1}$$

$$i_{pri}(t) = \frac{1}{n_1} i_o(t) \tag{2}$$

$$i_o(t) = \frac{(V_{S(1)} - V_o)}{L_o} + i(t_0), \quad (V_{S(1)} \rangle V_o) \tag{3}$$

Mode 2(t_1~t_2) : At time t_1, sub-switch S1 is turned off and its output capacitor C_{S1} is charged from 0V to V_{in} while the output capacitor of the sub-switch S2 is discharged form V_{in} to 0V. Because the energy is large enough to charge / discharge, the capacitor voltage of sub-switches is linearly increasing and decreasing. Also the sub-transformer voltage is decrease to zero along with the capacitor voltage V_{Cs2}.

$$V_{C_{s1}} = \frac{\frac{1}{n} i_{pri}(t_1)}{C_{S1} + C_{S2}} (t - t_1) \tag{4}$$

$$V_{C_{s2}} = V_{pri(2)} = V_{in} - \frac{\frac{1}{n} i_{pri}(t_1)}{C_{S1} + C_{S2}} (t - t_1) \tag{5}$$

Mode 3(t_2~t_3) : After V_{Cs2} is discharged to 0V in mode2(V_{Cs1} is charged to V_{in}), the reflected primary current $i_{pri(2)}$ flows through the body diode of the sub-switch S2. At this time V_{Cs2} and the sub-transformer voltage is sustained to 0V and the main-transformer primary voltage is $V_{in}/2$.

Mode 4(t_3~t_4) : The sub-switch S2 is turned on at time t_3. Since V_{Cs2} is 0V, S2 is turned on under ZVS condition. In this mode primary current decrease following the output inductor current. The primary current i_{pri} is expressed as follows;

$$i_{pri}(t) = \frac{1}{n_1} i_o(t) \tag{6}$$

$$i_o(t) = \frac{(V_{S(1)} - V_o)}{L_o} + i(t_3), \quad (V_{S(1)} \langle V_o) \tag{7}$$

Mode 5(t_4~t_5) : The main-switch M2 is turn-off at the beginning of this mode. The voltage of the output capacitor, C_{M2}, is linearly charged from 0V and the voltage of C_{M1} is linearly discharged from V_{in} at the same time by the large energy of output inductance. This mode continues until the time when the primary voltage of the transformer reaches to 0V.

$$V_{C_{M2}}(t) = \frac{i_{pri}(t_4) + \frac{1}{n_2} i_{pri}(t_4)}{C_{M1} + C_{M2}} (t - t_4) \tag{8}$$

$$V_{pri(1)}(t) = \frac{V_{in}}{2} - \left(V_{C_{M2}}(t) + \frac{1}{n_2} V_{C_{M2}}(t) \right) \tag{9}$$

Mode 6(t_5~t_6) : After the primary voltage of the main transformer reaches to 0V, the voltage of main-switch M2 increases in manner of resonance between L_{lkg} and 'C_{M1}+ C_{M2}. ' The voltage of M2 and the primary current are expressed as follows;

$$V_{C_{M2}}(t) = \left(i_{pri}(t_5) + \frac{1}{n_2} i_{pri}(t_5) \right) \sqrt{\frac{L_{lkg}}{C_{M1} + C_{M2}}} \sin\left(\sqrt{\frac{L_{lkg}}{C_{M1} + C_{M2}}} t \right) + V_{C_{M2}}(t_5) \tag{10}$$

$$i_{pri}(t) = i_{pri}(t_5) \cos\left(\sqrt{\frac{L_{lkg}}{C_{M1} + C_{M2}}} t \right) \tag{11}$$

In the secondary side, both rectifier diodes are conducted and commutation of the two diodes, D1 and D2, begin. This mode ends when the switch M1 voltage discharges to 0V.

Mode 7(t_6~t_7) : The primary current flows through the main-switch M1 whose voltage discharges completely in a previous mode. After the direction of the primary current is changed, the current flows through the body diode of M1. The primary current is expressed as;

$$i_{pri}(t) = -\frac{\frac{1}{2} V_{in} + \frac{1}{n_2} V_{in}}{L_{lkg}} (t - t_6) + i_{pri}(t_6) \tag{12}$$

This mode continues until following condition is satisfied;

$$n_1 i_{pri}(t) = i_{Lo}(t) \tag{13}$$

Mode 8(t_7~t_8) : When the reflected primary current reaches output inductor current, the secondary rectifier diodes finish its commutation. D2 is turned off and the secondary current flows through D1. Input energy is transfer to secondary side. The operation is similar to that of mode1.

3. Analysis of the Proposed Converter

In this section, DC conversion ratio, ZVS condition, offset of magnetizing current and output inductance are presented.

A. DC conversion ratio

The DC conversion ratio of the proposed converter can be expressed as follows;

$$\frac{V_O}{V_{in}} = \frac{2}{n_1} \times \left(\frac{D_{eff}}{n_2} + \frac{1}{4} \right) \quad (14)$$

(D_{eff} : the duration of mode1)

The DC conversion ratio of the proposed converter is first order equation, so that the variation depends on the input voltage variation is linearly changed.

B. ZVS condition

The proposed converter is able to have ZVS action(for main-switches) when it meets this condition:

$$\frac{1}{2}(C_{M1}+C_{M2}) \left(V_{in} - \frac{\frac{1}{2}V_{in}}{1+\frac{1}{n_2}} \right)^2 \le \frac{1}{2} L_{lkg} (i_{pri(1)} + \frac{i_{pri(1)}}{n_2})^2 \quad (15)$$

The sub-switches are well achieved ZVS condition using output inductor energy. For the main-switches, the output inductor is concerned until the time when main-transformer secondary side is shorted. Also the current which is reflected by the sub-transformer helps for ZVS of main switches.

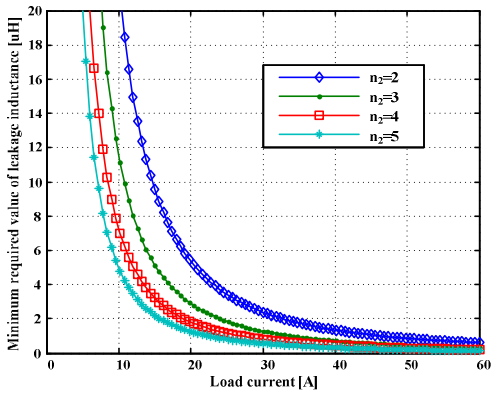

Fig. 4 The relation of the minimum required leakage inductance and load current(at 700W, Vo=12V spec.)

Fig. 4 shows the required leakage inductance on every load current condition. As load current increase, required leakage inductance for ZVS is decrease. The minimum required leakage inductance is also influenced by sub-transformer turn ratio. In a larger turn ratio, the better ZVS condition is achieved.

C. DC offset of magnetizing current

The DC offset of magnetizing current can be calculated by applying current-second law to C_2. It can be expressed as follows:

$$D_{eff}\left(I_{Lm} + \frac{I_O}{n_1} \right) = D_{eff}\left(-I_{Lm} + \frac{I_O}{n_1} \right) \quad (16)$$

$$\therefore I_{Lm,DC\,offset} = 0$$

D. Output inductance

In a conventional DC/DC converter, the output inductance can be calculated by following equation;

$$L_O = \frac{V_{Lo}}{\Delta I_O} DT \quad (17)$$

For the proposed converter, above equation is represented as:

$$L_O = \frac{\left(\frac{1}{2}V_{in} + \frac{1}{n_2}V_{in} \right)}{n_1} - V_O}{\Delta I_O} D_{eff} \frac{T}{2} \quad (18)$$

In a proposed converter, the frequency shown at the output filter inductor is twice higher than the switching frequency of the DC/DC converter..

4. Experimental Results

To verify the operation of the proposed converter, prototype circuit has been designed with following specifications : Input voltage : 400V(330V~400V). Output voltage/current : 12V/58A. Switching frequency : 86kHz. The magnetic cores used for the main transformer is EI3329 and for the sub-transformer is EI3026. The switches used in the primary side are SPP20N60C3. IRFB3077 switches are used for the synchronous rectifier switches in the secondary side. As shown in fig 5, the voltage of the main transformer is consisted of four different voltage level and there is no dc offset current in the primary current. Higher frequency of the output inductor current and ZVS switching characteristics are also the merits of the proposed converter.

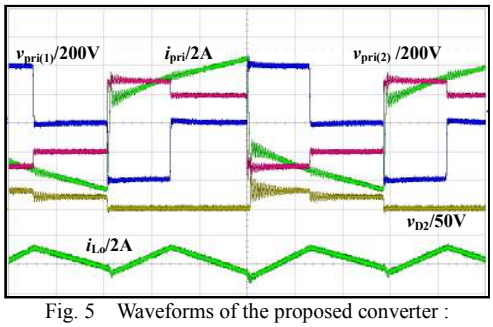

Fig. 5 Waveforms of the proposed converter : i_{pri}, $V_{pri(1)}$, $V_{pri(2)}$, V_{D2} and i_{Lo}

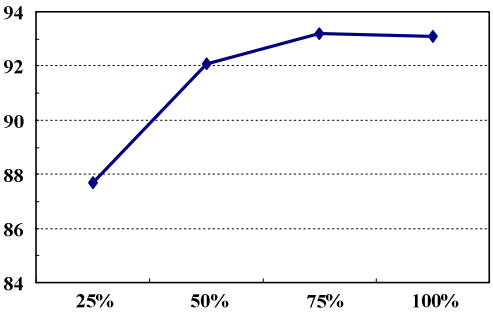

Fig. 6 Efficiency of the proposed converter

5. Conclusion

A new four level half-bridge converter is presented and analyzed. Even though the proposed circuit needs additional components, one small transformer and two small switches, it has low conduction loss, good ZVS condition and small output filter inductance. Furthermore, no DC offset characteristics helps to reduce the transformer size and distributes voltage / current stress symmetrically. The experimental results of the proposed converter prove the good performance of a new four level half-bridge converter.

Reference

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