Novel energy recovery circuit using an address voltage source

for high resolution and large-sized plasma display panels Kang-Hyun Yi and Gun-Woo Moon
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Abstract- Cost effective and high efficiency energy recovery circuit (ERC) using an address voltage source is proposed. Different from prior ERC, the proposed circuit uses a voltage source to charge a panel and a current source to discharge the panel. As a result, it can be achieved zero voltage switching (ZVS) of switches in H-bridge inverter and zero current switching (ZCS) of switches of the ERC. Moreover, the proposed ERC can obtain high efficiency, high performance and the decrease of the cost and the size.

I. INTRODUCTION

Plasma display panels (PDPs) are expected to be the best display for high definition (HD) television among flat panel display (FPD) due to wide view angel, large screen size, high contrast ratio, thinness and lightness. The PDP is operated with three steps of resetting, addressing and sustaining. Most of electrical power is consumed in sustaining period because a gray scale, brightness, is made by the number of sustaining pulse [1]. Since the PDP is regarded as a capacitive load (C_p), the EMI noise and considerable energy loss of $2C_pV_s^2$ for each cycle must be minimized by an energy recovery circuit (ERC) [2]. The well-known ERC is Weber & Wood circuit which has good features such as high efficiency and good flexibility. The Weber & Wood circuit has been employed by many PDP makers. Although the prior circuit is the most popular, it still has some undesirable drawbacks. First, when charging and discharging the PDP, parasitic components such as an equivalent series resistor (ESR) and a diode forward voltage drop prevent the panel fully charged to V_S and discharged to 0V. It resulted in hard switching operation in the all H-bridge inverter switches, an excessive surge current, serious power dissipation, EMI noise, and the undesirable voltage oscillation across the PDP. Second, energy recovery capacitors, C_1 and C_2, in Fig.1 are charged and discharged with large sinusoidal current in a high frequency. As a result, the considerable heat generated by an ESR of energy recovery capacitors would shorten their life-time. Therefore, several parallel-connected film capacitors with the low ESR must be used instead of electrolytic capacitor, which also increases the cost of production. As the large screen sized and high resolution PDP has been developed, the drawbacks could be serious. To overcome these drawbacks, a new ERC is proposed to get high power efficiency and to reduce the cost. The proposed circuit uses a voltage source to charge a panel and a current source to discharge the panel, so there are the zero voltage switching (ZVS) in main H-bridge inverter switches and the zero current switching (ZCS) in ERC switches. Since it uses an address voltage as a voltage source which is used during the addressing operation step, ERC capacitors can be removed and the remained current of ERC inductor can compensate the large gas discharge current in H-bridge inverter after charging the panel. Thus, the proposed ERC has high efficiency, simple structure and the low cost.

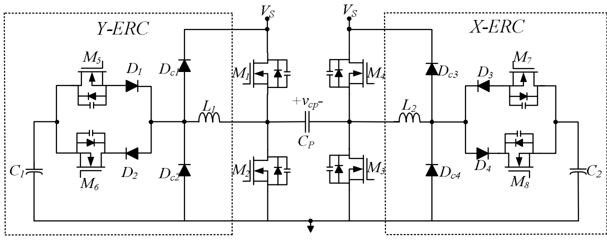


Fig. 1. Circuit diagram of the conventional ERC

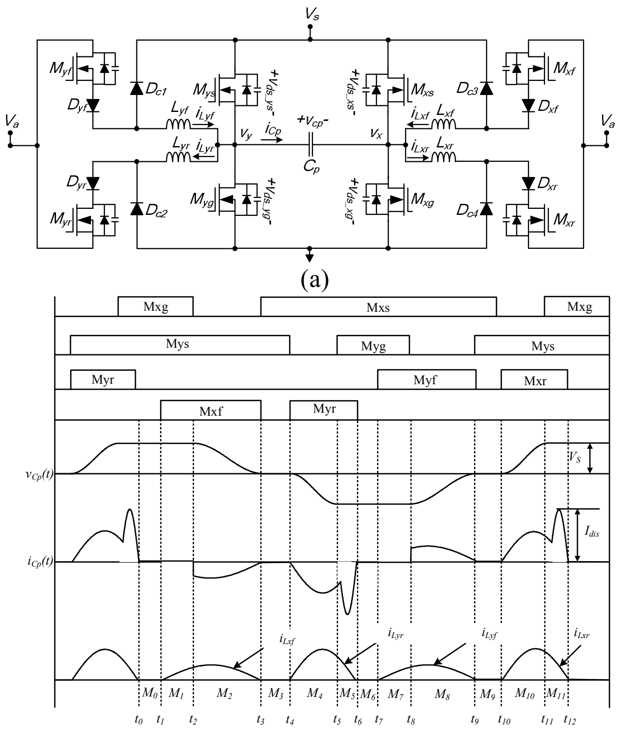
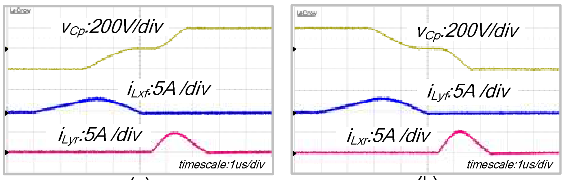


Fig. 2. Proposed circuit and its key waveforms (a) Circuit diagram of the proposed ERC (b) Key waveforms

II. PROPOSED ENERGY RECOVERY CIRCUIT

Fig. 2 shows a circuit diagram and key waveforms of the proposed ERC. The address voltage is used as energy recovery

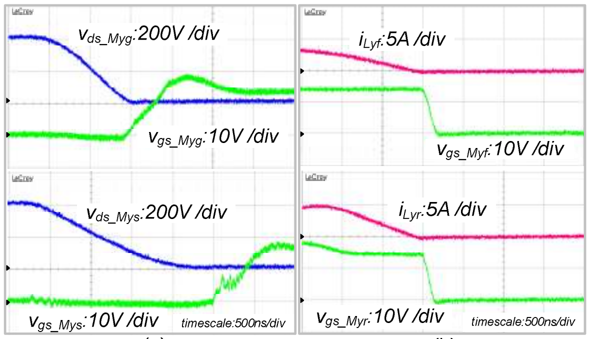


(a) (b)

Fig. 3 Experimental waveforms
(a) Panel voltage from $-V_S$ to V_S
(b) Panel voltage from V_S to $-V_S$

bias voltage source. To obtain different transition time of rising and falling, there are four inductors. An operational principle of the proposed circuit is explained as follows. It assumed that M_{ys} and M_{xg} have been turned on and the panel voltages, v_{cp}, is V_S at mode 0. The circuit operation has 12 modes, but since mode 0 ~ mode 5 and mode 6 ~ mode 11 are symmetric, mode 0 ~ mode 5 will be only considered. Mode 1 begins when M_{xf} is turned on at t_1. A current of L_{xf} is built up until t_2 with slope of $(V_S-V_a)/L_{xf}$. When M_{xg} is turned off, mode 2 begins. By a series resonance of panel capacitor C_p and inductor L_{xf} with the built up current and V_a bias voltage, the panel voltage, v_{cp}, is discharged to 0V until t_3. M_{xs} is turned on at t_3 and the panel voltage, v_{cp}, maintains 0V and this is mode 3. At this mode, the switch M_{xs} can be turned on the ZVS condition and the panel can be discharged to *0V* fully because the current source, $i_{Lxf}(t_2)$, can help the panel fully be discharged to *0*V without effect of parasitic components such as voltage drop of diodes, channel resistance of switches and the parasitic ESR. When M_{ys} is turned off and M_{yr} is turned on, mode 4 begins. At mode 4, the panel voltage can be charged to V_S by a series resonance of panel capacitor C_p and inductor L_{yr} with V_S -V_a voltage bias. After the panel voltage is charged to V_S, M_{yg} is turned on, the gas discharge can be occurred at mode 5. Since the voltage source is used, the panel voltage can be charged fully to *Vs* and M_{yg}, the switches of H-bridge inverter, can achieve the ZVS even if there are parasitic components. Moreover, the remained ERC inductor current, $i_{Lyr}(t_5)$, can be compensated the huge gas discharge current of main H-bridge inverter after the panel is charged to *Vs*. When the remained current of L_{xr} is decreased to zero, the mode 5 is finished. The ERC switch, M_{yr}, and diode D_{yr} can achieve the ZCS because those are turned off when the remained inductor current, i_{Lyr}, becomes zero at t_5.

Different from prior circuit, the panel voltage can be fully charged to *Vs* and discharged to 0V. So, the switches of H-bridge inverter can achieve the ZVS even if there are parasitic components. After charging and discharging the panel, the diodes and switches in ERC can be achieved the ZCS. In case of the ERC capacitor in the prior circuit, about fourteen or sixteen capacitors are used parallel because of the heat problem. However, ERC capacitors are removed in the proposed ERC. In addition, the power loss and heat dissipation in ERC devices can be improved by dividing the ERC current path. Moreover, root mean square (RMS) current value of the falling ERC inductors, L_{yf} and L_{xf}, can be smaller. As a result, the power consumption in D_{yf}, D_{xf}, M_{yf} and M_{xf} will be reduced. Therefore, the proposed ERC has higher efficiency, better performance, smaller size and less cost.



(a) (b)

Fig. 4 Waveforms of the soft switching
(a) The ZVS in the main inverter switches
(b)The ZCS in the ERC switches

III. Design consideration

To reduce the reactive power loss and to obtain good gas discharge uniformity, inductances of L_{yr}, L_{xr}, L_{yf} and L_{xf} are designed by considering the rising and the falling time of sustaining pulse. To obtain the desired rising time T_r (t_4~t_5=t_{10}~t_{11}) and falling time T_f (t_2~t_3= t_8~t_9), the inductors are selected as follows:

$$L_{yr}=L_{xr}=\frac{1}{C_p}\left(\frac{T_r}{cos^{-1}\left[1\text{-}V_S/\left(V_S\text{-}V_a\right)\right]}\right)^2$$

$$L_{xf}=L_{yf}=\left[T_f\,/\left[\sin^{-1}\left(V_a\,/\sqrt{V_a^2+(V_S\delta T\,/\sqrt{L_{yf}Cp})^2}\right)+\theta\right]\right]^2/\,C_p$$

where δT (t_1~t_2= t_7~t_8) and $\theta=\tan^{-1}(\sqrt{L_{yf}C_P}\,/\,\delta T)$.

IV. Experimental results

An experiment of the proposed circuit for verifying operation is performed with a 42-inch PDP which has about 80nF of a panel capacitance, C_p, in 200V sustaining voltage and 70V address voltage at 50 kHz. Components are in this circuit as follow: the H-bridge switches M_{ys}, M_{yg}, M_{xs} and M_{xg}: IXYS63N25, the M_{yr}, M_{yf} , M_{xs} and M_{xf}: IXYS63N25, diodes: 30CPF06, the inductor L_{yr}=L_{xr} for $T_r=1\mu s$: $9\mu H$, the inductor L_{yf}=L_{xf} for $T_f=2\mu s$: $45\mu H$. Fig. 3 and Fig.4 show experimental results. As can be seen in Fig. 3, the v_{cp} is charged and discharged, fully. In addition, it shows that peak values of i_{Lyf} and i_{Lxf} for the a slope of falling is smaller than those of i_{Lyr} and i_{Lxr} for a slope of rising due to (L_{yf}=L_{xf})$\leqslant$ (L_{yr}=L_{xr}). Fig. 4 shows waveforms of soft switching in the H-bridge inverter switches and the ERC switches. As you can see in Fig. 4, the switches in H-bridge inverter achieve the ZVS and those in the ERC also do the ZCS. Fig. 5 shows the comparison of the energy recovery efficiency, which means the power efficiency of the ERC. As expected, the proposed ERC has better performance than the conventional ERC. It shows the experimental waveforms are coincided with the theoretical key waveforms.

V. Conclusion

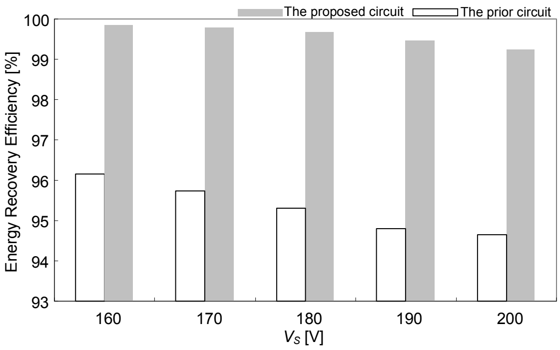


Fig. 5 Comparison of the energy recovery efficiency

The cost effective and high performance ERC has been proposed in this paper. The proposed ERC has used two sources like the voltage source and the current source to perform energy recovery. So, different from prior circuit, the panel voltage can be fully charged to V_S and discharged to 0V. The switches of H-bridge inverter can achieve the ZVS even if the parasitic components exist. Even though the current source is used for discharging the panel, the ERC devices can be turned off on the ZCS condition. Moreover, it has the low cost due to no ERC capacitors and can obtain high efficiency and performance of the ERC devices by dividing recovery path with the different transition time. Therefore, the proposed circuit can be expected to be suitable as an ERC for the high resolution and large-sized PDP TVs.

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