

A New Frequency Controlled Half-bridge Converter with Hold-up Time Extension Circuit

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Abstract

Hold-up time is a special requirement for the front end DC/DC converter in a server power supply. It forces the converter with the variable switching frequency to operate in a wide switching frequency range, which makes the regulation difficult and reduces the power density. In this paper a novel frequency controlled half bridge converter with the hold-up time extension circuit is proposed. During the hold-up time, the auxiliary switches are turned on, thus the resonant inductance is reduced and the voltage conversion ratio is increased. Therefore, the output capacitor of the power factor correction (PFC) circuit can be decreased, and the converter can have high power density. The proposed converter is verified by experimental results from a prototype with 700W, 400V input, and 12V output.

1. Introduction

Recently, the market of a server power supply has been increased, thus high efficiency and high power density are required for server power supplies. Also, it requires the hold-up time specification. During the hold-up time, the output voltage have to be maintained at desired value for more than 20ms after AC input line drops.[1][2]

The half-bridge (HB) converter is an attractive topology for medium-to-high power conversion because of its simplicity. There are two conventional control schemes for HB converter: symmetric control and asymmetric control.[3] The symmetric controlled HB converter has balanced voltage and current stresses of the switches and diodes. The main drawback of the symmetric control is that the primary switches operate at the hard switching condition. The asymmetrical controlled HB converter can be achieved the zero-voltage-switching (ZVS). However, because of the unbalanced voltage and current stress of the semiconductors, and magnetizing offset current, it is not suitable for wide input voltage applications.

Additionally there is the LLC resonant HB converter controlled by variable switching frequency method not pulse width modulation (PWM) method. This converter has features such as ZVS turn on of MOSFETs is achieved.[4] However, in high current application, the current stress of the secondary rectifier is very large because there is no output inductor.

In this paper, a new frequency controlled half-bridge converter with hold-up time extension circuit is proposed. The proposed converter can be controlled in variable switching frequency method like LLC resonant converter. Also the converter has an output inductor to reduce current stresses of the secondary rectifiers. Also, it has the additional two hold-up time switches. During the hold-up time, as two auxiliary switches are turned on, the frequency variation can be reduced.

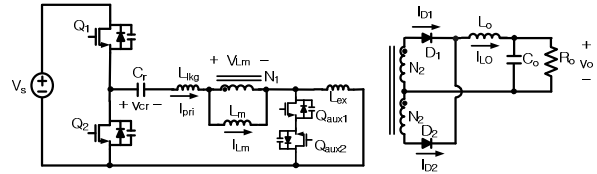


Fig. 1. The Schematic of the proposed converter

2. Operational Principles

Fig. 1 shows the circuit diagram of the proposed converter. The primary side of the proposed converter consists of two primary switches, transformer, resonant capacitor, external inductor, and two auxiliary switches. The duty ratio of the primary switches is fixed to 0.5, and the switching frequency is variable. The auxiliary switches are turned off during normal operation, and turned on during hold-up time.

Fig. 2 shows the key operating waveforms of the proposed converter. The waveforms of normal operation and that of hold-up time are same, so that only normal operation is explained. The operational principle is similar to the conventional half-bridge converter except for resonance between the resonant capacitor C_r and resonant inductor $L_m + L_{lk} + L_{ex}$. One switching cycle of the proposed converter can be divided into four modes. Since the operational principles of two half cycles are symmetric, only the half cycle is explained. A half cycle can be divided into two modes, powering mode and commutation mode, and their topological stages are shown in Fig 3. For the convenience of the analysis of the steady state operation, several assumptions are made as follows:

- $Q_1, Q_2, Q_{aux1}, Q_{aux2}$ are ideal except for output capacitors, $C_{oss1} = C_{oss2}, C_{oss_aux1} = C_{oss_aux2}$, and internal diodes.
- All parasitic components of the transformer except for the magnetizing inductor and the leakage inductor are neglected.
- The output filter inductance is large enough to be treated as a constant current source during switching period.
- The resonant capacitor is large enough to restrict the voltage variation within 0V to V_s .
- Turns ratio of the transformer is $n = N_2/N_1$.

Mode 1 [t_0-t_1] : Mode 1, powering period, begins when the commutation of secondary diode current is completed. Then D_1 is turned on. Since Q_1 is on state, Q_2 is off state, $V_s - v_{cr}$ is applied to $L_m + L_{lk} + L_{ex}$. The current flowing through L_m and L_{lk} can be expressed as follow:

$$i_{pri}(t) = C_r \frac{dv_{cr}(t)}{dt} = nI_o + i_{Lm}(t). \quad (1)$$

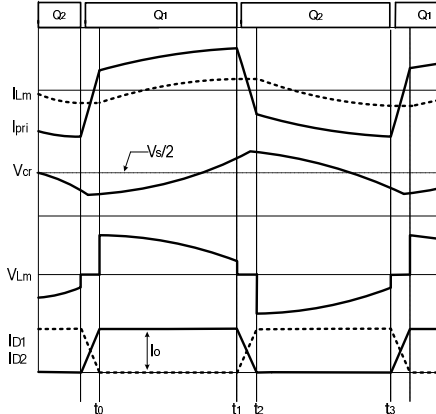


Fig. 2. The key waveforms of the proposed converter

$$i_{L_m}(t) = \frac{1}{L_m} \int_{t_0}^t (V_s - v_{cr}(\tau)) \frac{L_m}{L_m + L_{lk_g} + L_{ex}} d\tau + i_{L_m}(t_0). \quad (2)$$

Mode 2 [t_1 - t_2]: When Q_1 is turned off, this mode begins. The ZVS of Q_2 is achieved, the voltage across $L_m + L_{lk_g} + L_{ex}$ changes to $-v_{cr}$. And that, the commutation of the load current from D_1 to D_2 occurs. During this mode, the voltage across L_m is 0V, $-v_{cr}$ is applied to $L_{lk_g} + L_{ex}$. The slope of the current can be expressed as follows:

$$\frac{di_{pri}(t)}{dt} = \frac{-v_{cr}(t)}{L_{lk_g} + L_{ex}}. \quad (3)$$

When the commutation is completed, this mode ends.

3. Analysis of the Proposed Converter

3.1 Normal operation and Hold-up time

During hold-up time, the proposed converter regulates the output voltage with lower input voltage at same frequency than normal operation. Since during hold-up time, the resonant inductance changes from $L_{lk_g} + L_{ex}$ to L_{lk_g} , the voltage conversion ratio is increased. Fig. 4 shows the concept of the proposed circuit. When the switching frequency swings from F_1 to F_2 , the voltage conversion of the conventional converter, which has no auxiliary switches, swings from G_1 to G_2 . In case of the proposed converter, when the input voltage drops, the auxiliary switches are turned on, and the voltage conversion ratio can be increased to G_3 . From the below equation, the lower input voltage the converter can be regulated with, the smaller PFC output capacitor can be.

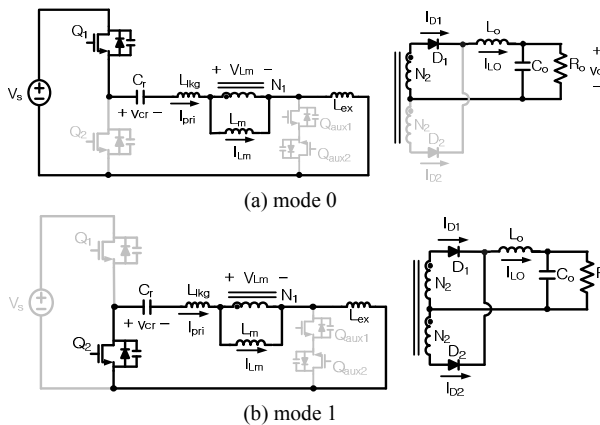


Fig. 3. The equivalent circuit of the proposed converter

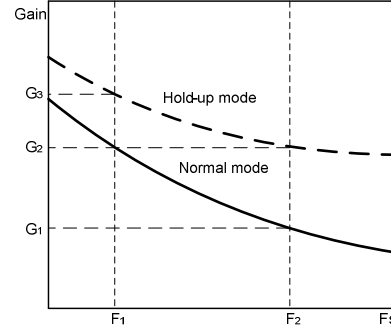


Fig. 4. The voltage conversion ratio vs. switching frequency

$$C_{PFC_OUT} = \frac{2P_{in} \Delta t_{holdup}}{V_{nom}^2 - V_{min}^2}. \quad (4)$$

P_{in} is input power, Δt_{holdup} is hold-up time, V_{nom} is DC/DC nominal input voltage, and V_{min} is DC/DC minimum input voltage.

3.2 Voltage Conversion Ratio

The voltage conversion ratio of the proposed converter is given by

$$V_o = \frac{2n}{\omega T_s} \left(\frac{L_m}{L_m + L_r} \right) V_s \tan \omega \left(\frac{T_s}{4} - \frac{T_{dead}}{2} \right). \quad (5)$$

In this equation, T_s is switching period, L_r is $L_{lk_g} + L_{ex}$ at normal operation and L_{lk_g} at hold-up time, $\omega = 1/\sqrt{C_r(L_m + L_r)}$, and T_{dead} is the time interval of the commutation period. With the assumption that v_{cr} is linear and primary current is nI_o as shown in Fig. 5, T_{dead} can be calculated as follows:

$$\begin{aligned} \frac{1}{2} \Delta v_{cr}^2 + \left(V_{cr} - \frac{1}{4C_r} nI_o T_s \right) \Delta v_{cr} \\ + \frac{2}{C_r} n^2 I_o^2 L_r - \frac{V_{cr}}{2C_r} nI_o T_s = 0. \end{aligned} \quad (6)$$

$$\frac{1}{L_r} \left(V_{cr} + \frac{\Delta v_{cr}}{2} \right) T_{dead} = 2nI_o, \quad (7)$$

where V_{cr} is $V_s/2$.

3.3 Turns Ratio of the Transformer

With the above equation (5), the turns ratio of the transformer can be determined.

$$n = \frac{V_o}{2V_s} \left(\frac{L_m}{L_m + L_r} \right) \omega T_s / \tan(\omega T_s / 4 - T_{dead} / 2). \quad (8)$$

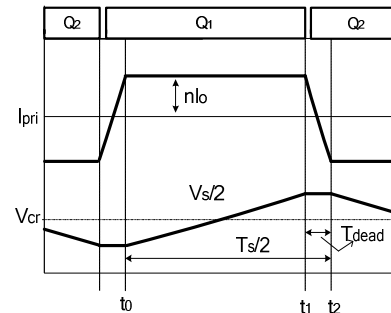


Fig. 5. The key waveforms of current and voltage across the resonant capacitor

Table 1. Parameters of the prototype circuit

Item	Symbol	Value/Part
Nominal Input Voltage	V_{in}	400V
Output Voltage	V_o	12V
Max. Power Rating	P_{max}	700W
Switching Frequency	F_s	60~130kHz
Turn Ratio	$N_1:N_2$	16:1
Leakage inductance	L_{lk}	7uH
External inductance	L_{ex}	17uH
Magnetizing inductance	L_m	300uH
Resonant Capacitance	C_r	120nF
Output Capacitance	C_o	470uF
Output inductance	L_o	5uH

3.4 Resonant Capacitor

With the assumption that the voltage across the resonant capacitor is linear, the voltage variation of the resonant capacitor is given by

$$\Delta v_{cr} = \frac{1}{C_r} \int i_{cr} dt = \frac{1}{C_r} n I_o \frac{T_s}{2} \quad (9)$$

To limit the range of the voltage across the capacitor from 0V to V_s in any condition, the resonant capacitance is determined by as follow:

$$C_r > \frac{n I_o T_{s_max}}{2 V_{s_min}} \quad (10)$$

4. Simulation Results

In order to verify the operation of the proposed converter, a 700W converter was simulated by PSIM program. The parameters of this simulated circuit are listed in Table 1. Table 2 shows that the input voltage can be decreased with the auxiliary switches. Therefore, with the above equation (10), 921uF is used for the output capacitor of PFC circuit without auxiliary switches, however, it can be decreased to 486uF with auxiliary switches.

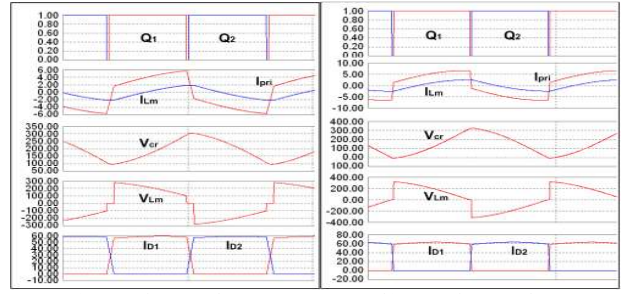
Fig. 6 (a) shows simulated key waveforms of the proposed converter when the input voltage is 400V (normal operation), and Fig. 6 (b) shows when the input voltage is 320V (hold-up time). Due to the small magnetizing inductance the ZVS operation of the main switches is easily achieved even 10% load as shown in Fig. 7.

5. Conclusion

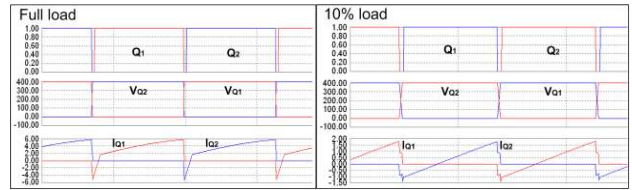
This paper presents the analysis and experimental results of the new frequency controlled half-bridge converter with hold-up time extension circuit. Since the duty ratio is fixed at 0.5 and magnetizing inductance is small, there is no L_m DC current offset and it has wide ZVS range. During hold-up time, the voltage gain is increased with turning on the auxiliary switches. Thus, it can

Table 2. Input voltage versus switching frequency

Aux. Switches State	Switching Frequency	Load Condition	Voltage Gain	Input Voltage
Off (normal)	60kHz	Full load	0.0333	360V
	130kHz	1% load	0.03	400V
On (hold-up)	60kHz	Full load	0.0375	320V
	120kHz	1% load	0.0333	360V



(a) 400V input voltage (b) 320V input voltage
Fig. 6. The key waveforms of the simulated circuit



(a) Full load (b) 10% load
Fig. 7. ZVS of Q_1 and Q_2 (a) at full load, (b) at 10% load

operate with lower input voltage, and output capacitor of PFC circuit can be smaller. Therefore, the proposed converter is suitable for high efficiency and high power efficiency in the server power supply application.

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