Single-Phase Z-Source AC-AC Converter (SZAC) with Buck/Boost In-Phase

and Out-Of-Phase Operation

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Abstract

A new family of single-phase Z-source ac-ac converter(SZAC) based on single-phase matrix converter (SPMC) is proposed in this paper. Compared to conventional Z-source ac-ac converter, the proposed SZAC has unique feature: providing a wide range of output ac voltage with buck/boost in-phase (maintaining phase angle) and buck/boost out-of-phase (reversing phase angle) operation. A new commutation strategy is used to eliminate voltage spikes on switches. The operating principle of the proposed SZAC is presented. Analysis and experimental results are also presented.

1. INTRODUCTION

Single-phase Z-source ac-ac converters proposed in [1] have the following features: providing a larger range of output voltage with buck-boost, reversing or maintaining phase angle, reducing in-rush and harmonic current. But they do not provide safecommutation paths. In other to solve commutation problem, a family of single-phase four switches structure Z-source ac-ac converter topologies with commutation strategy is presented in [2] which achieved high efficiency and reliability. In the conventional single-phase Z-source ac-ac converters proposed in [1,2], however, the output voltage cannot be bucked, and in-phase with input voltage.

In order to overcome this problem, a new family of singlephase Z-source ac-ac converter(SZAC) based on SPMC topology [5] is proposed in this paper. Compared to the existing PWM ac-ac converters, the proposed SZAC can provide a wide range of output ac voltage operation region. A commutation technique which is very simple to implement is used as free-wheeling path to provide the required free-wheeling operation similar to those available in other converter topologies. The commutation scheme establishes a continuous current path in dead time to eliminate voltage spikes on switches. The operating principle, analysis and experiment of the proposed SZAC are presented.

2. THE PROPOSED SYSTEM

Fig. 1 shows the proposed single-phase Z-source ac-ac voltage-fed converter. It employs a Z-network, bi-directional switches, $L_f C_f$ output filter and *R* load. The symmetrical Z-network, a combination of two inductors and two capacitors, is the energy storage/filtering element for the proposed SZAC. Since the switching frequency is much higher than the ac input source frequency, the inductor and capacitor requirement should be low [1]. As shown in Fig. 1, the proposed SZAC requires four bi-

directional switches S_{1j} , S_{2j} , S_{3j} , S_{4j} (j = a, b) as SPMC and one source bi-directional switches S_{sj} (j = a, b), where 'a' and 'b' are representing drivers one and two, respectively. All bi-directional switches are common emitter back to back switch cells.



3. SWITCHING STRATEGY SOLVING THE COMMUTATION PROBLEM

3.1 Commutation Problem

Five bi-directional switches S_{sj} , S_{1j} , S_{2j} , S_{3j} , S_{4j} (j = a, b) are able to block voltage and conduct current in both directions. Because the bi-directional switches are not available to date, they can be implemented by connection of two diodes and two IGBTs in anti-parallel (common emitter back to back) as shown in Fig. 1 [3,6]. The commutation problem appears when active components such as inductor, capacitor are used. A change in current due to PWM switching will result in current and voltage spikes being generated resulting in the occurrence of a dual situation. First current spikes will be generated in the short circuit or shootthrough path and secondly voltage spikes will be induced as a result of change in current direction across the inductance. Both will destroy the switches because of stress [3]. Previous method is usually adding lossy snubber circuit for each switch to limit voltage overshoot. In addition, it provides commutation paths in dead time which results in inefficient and unreliable.

3.2 Operating Principles

For the proposed SZAC topology, take the voltage-fed converter topology shown in Fig. 1. Fig. 2 shows the switching strategy for the proposed SZAC in buck/boost out-of-phase operation. The operation of the proposed SZAC can be divided into two stages.

Stage 1: $(v_i(t) > 0)$. The switches S_{sb} , S_{2b} , S_{3a} , and S_{4a} are fully turned on $(S_{4a}$ turns on for commutation purpose; S_{sb} and S_{2b} turn on for continuous current flow purpose); S_{sa} , S_{1b} and S_{2a} are modulated in complement with dead time. In state 1, as shown in Fig. 1, S_{sa} and S_{2a} turn on and conduct current flow during positive cycle of input voltage; S_{4a} turns on for commutation purpose. Then S_{2a} and S_{sa} turn off and S_{Ib} has not turned on, there are two occurring commutation states. If $i_{L1} + i_{L2} + i_{Lf} > 0$, the current path flows from S_{2b} and S_{4a} as shown in Fig. 1; if $i_{L1} + i_{L2} + i_{Lf} < 0$, the current path flows from S_{4b} , as shown in Fig. 1. In state 2, as shown in Fig. 1, S_{1b} turns on and conduct current flow in Z-source network as shoot-through path; the load current may be freewheeled through S_{4a} , S_{3a} . In these switching patterns, the current path is always continuous whatever the current direction. Thus, the voltage spikes are eliminated during switching and commutation processes.

Stage 2: $(v_i(t) < 0)$. The switches S_{sa} , S_{1b} , S_{2b} , and S_{3a} are fully turned on $(S_{1b}$ turns on for commutation purpose; S_{sa} and S_{3a} turn on for continuous current flow purpose); S_{sb} , S_{3b} and S_{4a} are modulated in complement with dead time. In state 1, as shown in Fig. 1, S_{sb} and S_{3b} turn on and conduct current flow during negative cycle of input voltage; S_{1b} turns on for commutation purpose. In state 2, as shown in Fig. 1, S_{4a} turns on and conduct current flow in Z-source network as shoot-through path; the load current may be freewheeled through S_{1b} , S_{2b} . The analysis of commutation states in stage 2 is similar to that in stage 1.

The operation of other regions is similar to that in buck in-phase operation region as analyzed above.



Fig. 2 Switching safe-commutation strategy of the proposed SZAC(buck/boost out-of-phase operation)

Let D is an equivalent duty-ratio; T is a switching period, the voltage gain (K) can be defined as

$$K = \frac{v_R}{v_i} = -\frac{D}{2D-1}; D < 0.5:$$
 region (I)

$$\begin{bmatrix} K = \frac{v_R}{v_i} = \frac{D}{2D - 1}; D > 0.5: & \text{region (II)} \\ K = \frac{v_R}{2D - 1}; D < 0.5: & \text{region (III)} \end{bmatrix}$$
(1)

$$K = \frac{v_i}{v_i} = -\frac{D}{2D-1}; D > 0.5:$$
 region (IV)

Fig. 3 shows the voltage gain versus the duty cycle. As shown in Fig. 3, when D is less than 0.5, the converter can be bucked or boosted in-phase. We can divide the duty cycle into two parts, D =[0, 0.33] is for buck mode, and D = [0.33, 0.5] is for boost mode. The proposed SZAC has four operating regions. When D is less than 0.33, region (I) and (III) are called buck in-phase and buck out-of-phase, respectively; and when D is greater than 0.5, region (II) and (IV) are called boost in-phase and boost out-of-phase, respectively as shown in Fig. 3.



Fig. 3 Voltage gain (K) versus duty cycle (D) with wide range output voltage gain operation capability

4. EXPERIMENTAL RESULTS

Experiment is implemented for the proposed topology at V_i = 40Vrms(56Vpeak)/60Hz. The system parameters were used as shown in table 1.

Table 1 Experimental Farameters		
	$L_1 = L_2$	1 mH
Z-network	$C_1 = C_2$	1 μF
	c_2	
Switching frequency		20 kHz
Dead time		0.5 μs
Duty cycle (D)		0.25, 0.7
	L_{f}	3 mH
Output filter	C_{f}	3.3 µF
Load (R)		50 Ω

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Fig. 4 shows the experimental results with various operation regions in Fig.3. In case the operation region is buck in-phase mode as shown in Fig. 4(a), the experimental result shows that the output voltage was bucked to $V_o = 13$ Vrms(19Vpeak) from $V_i = 40$ Vrms(56Vpeak). In addition, the output voltage is in-phase as shown in Fig. 4(a) or 180° out-of-phase as shown in Fig. 4(b) with the input voltage. In case the converter operates in boost mode as shown in Fig. 5, experimental results show that when D = 0.7, output voltage is boosted to $V_o = 52$ Vrms(74Vpeak) from $V_i = 40$ Vrms(56Vpeak). In addition, the output voltage is in-phase as shown in Fig. 5(a) or 180° out-of-phase as shown in Fig. 5(b) with the input voltage.

By experimental results, we can observe that the proposed SZAC can provide a wide range output voltage operation. The output voltage can be bucked or boosted. In addition, the output voltage can be in-phase or 180° out-of-phase with the input voltage depending on operation regions of the duty cycle D.



(b) Region (III) (buck out-of-phase)

Fig. 4 Experimental results of buck-mode at D = 0.25 (From top to bottom: v_i , v_{Cl} , v_R , i_R) (50V/div., 1A/div., 10ms/div.)



(a) Region (II) (boost in-phase)



Fig. 5 Experimental results of boost-mode at D = 0.7 (From top to bottom: v_i , v_{Cl} , v_R , i_R) (100V/div., 2A/div., 10ms/div.)

5. CONCLUSIONS

In this paper, a new family of single-phase Z-source ac-ac converter(SZAC) based on SPMC topology was proposed. The proposed topology provides a wide range output voltage operation. By duty-ratio control, the proposed converter becomes "solid-state transformers" with a continuously variable turns ratio. The proposed SZAC can be used for ac-ac line conditioning to overcome voltage sags, surges, and load fluctuations. In order to provide a continuous current path, the safe-commutation strategy is employed. Steady-state analysis and experimental results were illustrated. From the proposed SZAC based on SPMC topology, further research can be implemented for variable output frequencies by changing switching scheme without reset up experimental system configuration. Thus, the proposed SZAC can be also called an amplitude voltage step-up/down and frequency step-up/down converter.

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