LLC Resonant Converter with Hold-up Time Extension Technique for Computer Power Supply

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Abstract

A LLC resonant converter with hold-up time extension technique for computer power supply is proposed. Since the proposed circuit has a current boost-up capability of resonant inductor regardless of the input voltage level and the load power condition, operating near the resonant frequency, it can provide the power to the load as the input voltage drops to half of reflected output voltage to the transformer primary. This extends the hold-up time of computer power supply and improves the system power density and conversion efficiency at nominal input voltage. The experimental results with prototype are given to confirm the validity of the proposed circuit.

1. Introduction

With the development of power conversion technology, the power density of converter has become the major challenge. In the computer power supply application, the size of link capacitor, which is placed between front-end AC/DC and back-end DC/DC converter as shown in Fig. 1 and store the energy that is used to deliver power to the load for a short time (typically 10~20 ms) after a line dropout, becomes a important factor for high power density. To minimize the hold-up-time capacitor, different research efforts have been proposed, by using extra hold-up time extension circuit or by developing better topologies [1]-[4]. In the hold-up time extension circuit approach, the improved utilization of the stored link-capacitor energy is obtained by employing an additional boost-type converter, which is unaffected to the performance and control of DC/DC conversion stage [1], [2]. But, since its implementation requires additional bulk inductor, there is a limitation to achieve attainable power density. On the other hand, in the development approach of better topologies for hold-up-time extension, LLC resonant converter is the most attractive topology due to its high efficiency and wide operation range [3],[4]. Fig. 2a shows circuit diagram of conventional LLC resonant converter and Fig. 2b is the plot of its simplified voltage gain obtained by the fundamental element simplification. This simplified DC voltage gain function can be expressed as follows.

$$G_{dc} = |G_{ac}|/n = 1/n\sqrt{\left\{1+\frac{1}{L_n}\left[1-\left(\frac{F_R}{F_S}\right)^2\right]\right\}^2+\left[\left(\frac{F_S}{F_R}-\frac{F_R}{F_S}\right)\frac{\pi^2}{8}Q\right]^2} \qquad (1)$$

where $F_R = 1/2\pi\sqrt{L_r C_r}$, $Q = 4\sqrt{L_r/C_r}/n^2 R_O$, and $L_n = L_m/L_r$.

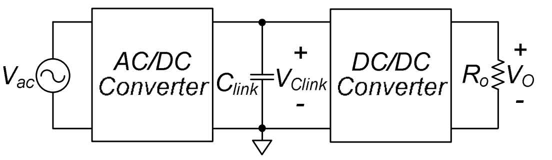
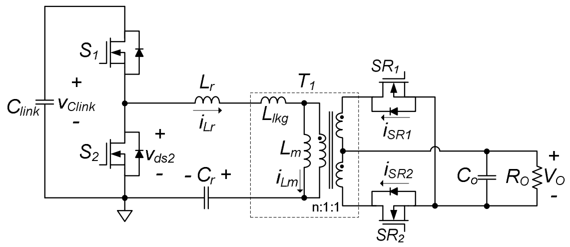
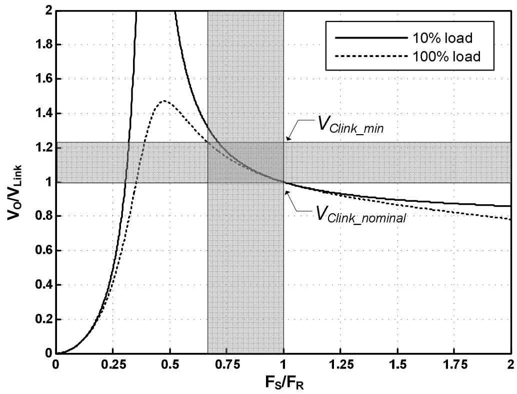


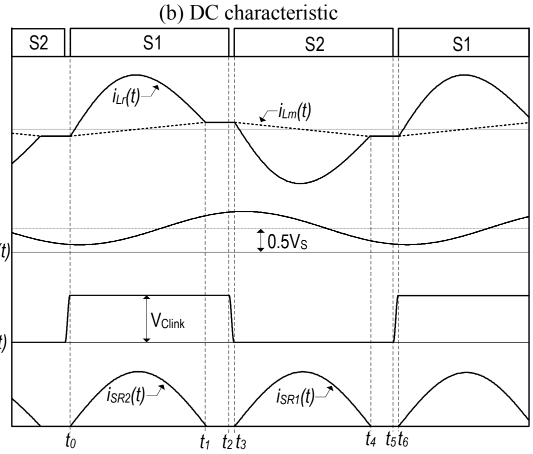
Fig. 1 Typical off-line ac-dc power supply



(a) Circuit diagram



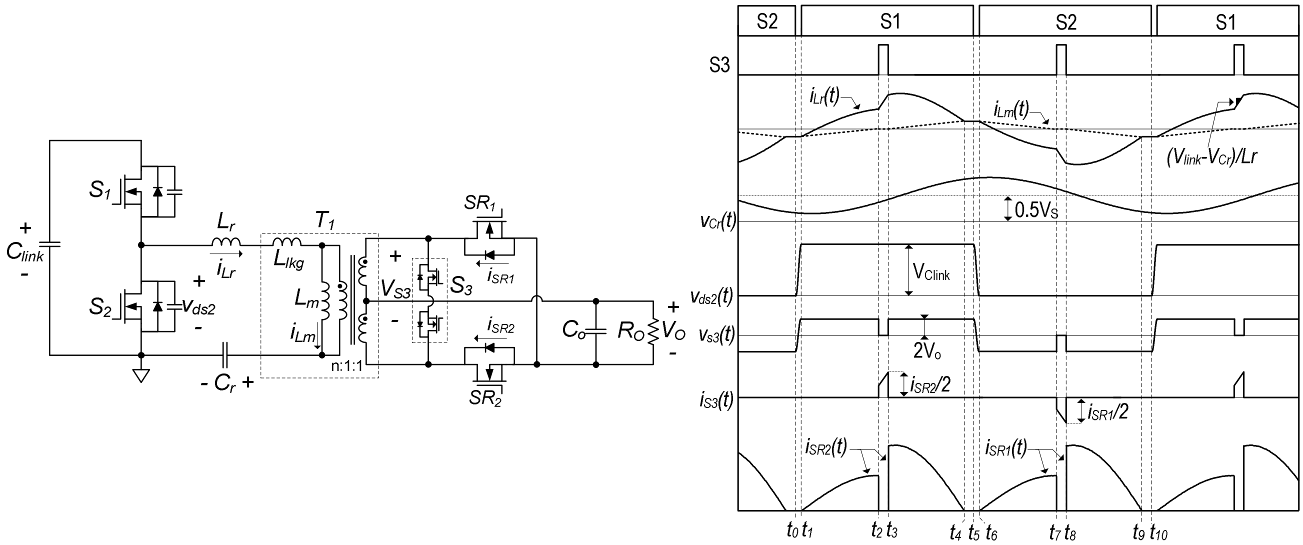
(b) DC characteristic



(c) Key operational waveforms

Fig. 2 Conventional LLC resonant converter

The operation below the resonant frequency, F_R, allows the zero voltage switching (ZVS) of primary power switches over the entire operating range and the soft commutation of the secondary rectifiers. It is very effective in improving efficiency for all the load condition. As can be seen from (1), the L_n and Q value could affect the gain characteristic of converter. This shows that the converter can be designed for obtaining an enough peak gain to cover the desired input voltage range, reducing the hold-up time capacitor requirement.



(a) Circuit diagram (b) Key operational waveforms

Fig. 3 Proposed converter and its key operational waveforms

Generally, the optimal operating point for this converter is known when operating frequency equals to the resonant frequency. Since the voltage gain of LLC resonant converter at this point is almost one over all the load condition, the transformer turn ratio can be chosen based on the nominal input voltage. The magnetizing inductance also can be designed to guarantee the zero voltage switching of main power switches, S_1 and S_2, at specific resonance frequency. But, to determine the resonant tank of L_r and C_r, lot of trade offs are involved because there are many values of L_n and Q to meet the hold-up time voltage gain requirement. In the literature presented in [6], the high L_n and low Q design shows that the switching loss and conduction loss can be minimized at nominal input voltage, but its performance degrades very fast as input voltage drops. This is because the operating frequency moves downward far from the resonant frequency. This results in large circulating current in the primary side and degrading the average efficiency over the entire input range. Therefore, considering the tradeoff of the power loss over the input range, the low L_n and high Q design is generally used.

To solve these problems, LLC resonant converter with hold-up time extension technique for computer power supply is proposed. Since the proposed circuit has a current boost-up capability of resonant inductor regardless of the input voltage level and the load power condition, operating near the resonant frequency, it can provide the power to the load as the input voltage drops to voltage across the resonant capacitor. Thus, proposed circuit extends the hold-up time of computer power supply and improves the system power density and conversion efficiency at nominal input voltage by adopting the high L_n and low Q design. To confirm the validity of the proposed circuit, the experimental results with prototype will be given.

2. Operational Principles

Fig. 3a shows the circuit diagram of the proposed circuit and Fig. 3b is its key operational waveforms during the hold-up time. As can be seen in Fig. 3a, the proposed circuit is identical to the conventional one, except for the bidirectional switch, S_3, in the transformer secondary side. By using this bidirectional switch, current boost-up capability of proposed circuit can be achieved. The operation of proposed circuit when the input voltage is nominal range is the same as those of conventional one. After input voltage line drops out, as the input voltage of the converter, namely the voltage across link capacitor, decreases linearly, the operating frequency of proposed circuit moves downward from the resonant frequency to regulate the output voltage. When the operating frequency reaches the specific minimum frequency, inductor current boost-up function of proposed circuit is initiated. As shown in Fig. 3b, one operational cycle of the proposed circuit is divided into two half cycles, t_0~t_5 and t_5~t_{10}. Since the operational principles of two half cycles are symmetric, only the first half cycle is explained. Before t_0, there is a resonance between L_r, L_m, and Cr as shown in Fig. 4a and no energy is transferred to the secondary side and output capacitor only provides power to the load.

Mode 1(t_0~t_1): Mode 1 begins when S_2 is turned off at t_0. At this moment, resonance consisted of L_r, L_m, C_r, and parasitic output capacitance of the primary power switches occurs as shown in Fig. 4b. This makes voltage across S_1 fully discharges to zero. The voltage across synchronous rectifier, SR_2, at the secondary side is also decreased to zero. After the v_{DS1} reaches to zero, resonant inductor current flows through the body diode of S_1 and secondary rectifier SR_2 is forward-biased.

Mode 2(t_1~t_2): At t_1, switch S_1 is turned on at ZVS condition. As can be seen in Fig. 4c, a series resonance between C_r and L_r occurs as follows:

$$i_{Lr}(t) = [V_{Clink} - V_{Cr}(t_1) - nV_o]\sin\omega(t-t_1)/Z_o - nV_o/2L_m f_S \quad (2)$$

$$v_{Cr}(t) = [V_{Clink} - V_{Cr}(t_1) - nV_o]\cos\omega(t-t_1) + v_{Cr}(t_1) \quad (3)$$

where $Z_o = \sqrt{L_r/C_r}$ and $\omega = 1/\sqrt{L_r C_r}$.

With this arrangement, input power is transferred to the secondary output. Meanwhile, reflected output voltage, nV_o, is applied across L_m and magnetizing current i_{Lm} keeps rising linearly as follows:

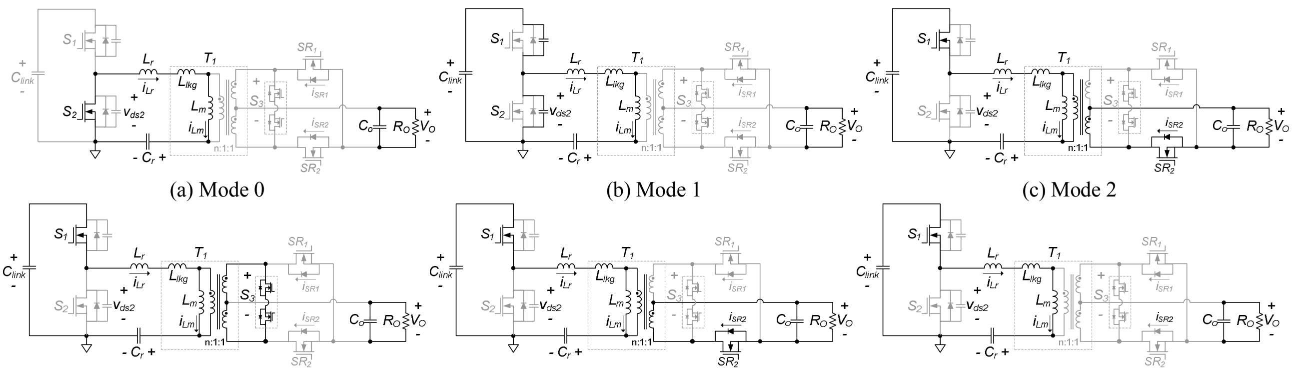
$$i_{Lm}(t) = nV_o(t-t_1)/L_m - nV_o/2L_m f_S \quad (4)$$

Mode 3(t_2~t_3): While switch S_1 is still turned on, bidirectional switch S_3 in the transformer secondary side is turned on at t_2. As shown in Fig. 4d, this makes the transformer short-circuit state and output voltage is ejected from bias of series resonance. Therefore, a series resonant condition is changed as follows:

$$i_{Lr}(t) = [V_{Clink} - V_{Cr}(t_2)]\sin\omega(t-t_2)/Z_o + i_{Lr}(t_2) \quad (5)$$

$$v_{Cr}(t) = [V_{Clink} - V_{Cr}(t_1)]\cos\omega(t-t_2) + v_{Cr}(t_2) \quad (6)$$

As can be seen these equations, resonant inductor current boosts up during this mode and boost-up capability of proposed circuit can be achieved until the input voltage drops to the voltage across the resonant capacitor. The magnetizing inductor is maintained to be $i_{Lm}(t_2)$ during this mode since the transformer is short-circuit state.



(a) Mode 0 (b) Mode 1 (c) Mode 2
(d) Mode 3 (e) Mode 4 (f) Mode 5

Fig. 4 Equivalent circuit of proposed converter for each mode

Mode 4(t_3~t_4): When switch S_3 is turned off and SR_2 begins conducting, mode 4 begins. As can be seen in Fig. 4e with a initial condition of $i_{Lr}(t_3)$, a series resonance between C_r and L_r occurs. With this arrangement, the input power is again sent to the secondary output. Also, the magnetizing current is again increased by reflected output voltage. When the current through secondary rectifier decreases to zero and SR_2 stops conducting, mode 4 ends.

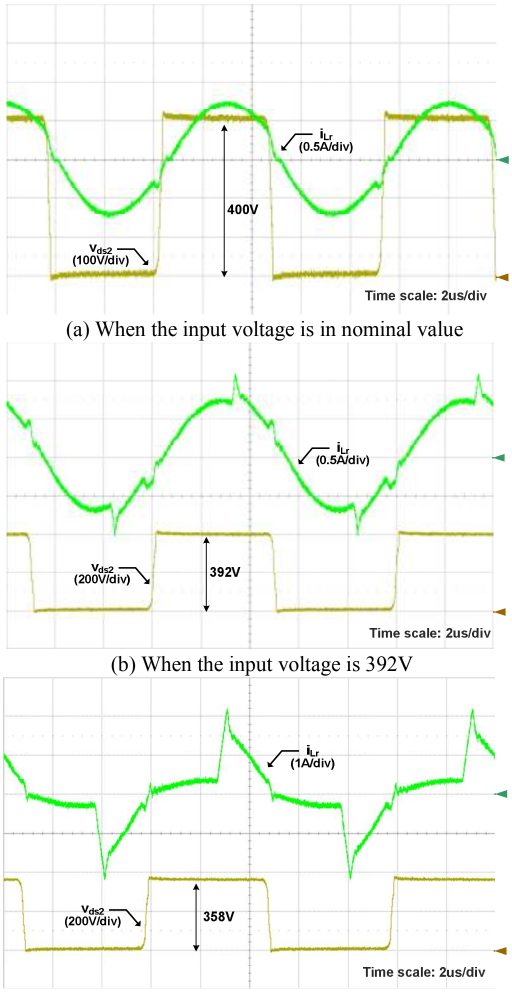
Mode 5(t_4~t_5): When the resonant current, i_{Lr}, is equal to the magnetizing current, i_{Lm}, mode 5 begins. During this mode, there is a resonance between L_r, L_m, and Cr and no energy is transferred to the secondary output.

3. Experimental Results

To confirm the validity of proposed converter, prototype with 100W and 12V output has been built. The resonant frequency is designed as 110 kHz. Fig. 5 shows the key experimental waveforms of the proposed circuit when the input voltage maintains nominal level and drops to minimum input voltage. As can be seen in these figures, when the input voltage maintains nominal level, operation of proposed circuit is the same as those of conventional one. As the input voltage decreases linearly, the boost-up function of resonant inductor is initiated, which . Therefore, despite of operating near the resonant frequency, the proposed circuit can regulate the output voltage.

4. Conclusion

The proposed converter provides hold-up time extension method for LLC resonant converter. The proposed circuit has a current boost-up function of resonant inductor by using bidirectional switch in the secondary side. This guarantees the LLC resonant converter operating near the resonant frequency regardless of the input voltage level and the load power condition during the hold-up time. Therefore, without significant efficiency degradation, proposed converter can extend the hold-up time of computer power supply.



(a) When the input voltage is in nominal value

(b) When the input voltage is 392V

(c) When the input voltage is 358V

Fig. 5 Experimental waveforms of proposed converter

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