Realization of Small Size Power Divider Chip for Dual Band Operation at 900/1800 MHz

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Abstract : In this paper the power divider is realized using the IPD processes for 900/1800 MHz; the designed power divider achieved the isolation of more than -24 dB, the insertion loss of nearly -3.5 dB, and the return loss of about -25 dB. The simple dual-band power divider based on SI-GaAs substrate is realized within the die size of about 2.5 × 2 mm^2.

Key Words : IPD, dual band, SI-GaAs, power divider

1. Introduction

Nowadays, power divider has attracted much attention in microwave communication systems, so it has been used for impedance matching, antenna polarization, and phase control in phased array antenna, for example, primarily due to the excellent isolation. Dual-band and Ka-band Wilkinson power dividers were designed and presented in recent years; they were designed and realized by hybrid MIC structures with lumped chips (R, L, and C), and their sizes were relatively huge [1],[2].

In this paper, the realization of a 900/1800 MHz dual band power divider IC chip based on IPD technology was proposed. The power divider has a compact size and good RF performances.

2. IPD Process

In this paper, RF passive devices (such as MIM capacitors, thin film resistors, high Q inductors) and a dual-band filter is implemented using SI-GaAs IPD process with 6 masks. Figure 1 presents a cross-sectional view of GaAs integrated passive devices. To achieve cost and size reductions, a low cost manufacturing technology for RF substrates and a high performance passive process technology are developed for RF-IPDs.

The substrate used for fabrication is a 6 inch SI-GaAs wafer, which is advantageous to avoid the capacitive and inductive loading of a conductive substrate [3], with thickness of 0.625 mm, permittivity of 12.85, and a loss tangent of 0.006. The process features two levels of plated Cu/Au metal; for the first metal with thicknesses of Cu 4.5 μm and Au 0.5 μm, for the second metal with thicknesses of Cu 3.0 μm and Au 2.0 μm. PECVD Si_3N_4 of 1000 Å was used as the capacitor dielectric layer. Air-bridges were used for the metal layer crossover between inductor windings and the underpasses. After thinning the wafer to its final thickness (200 μm), backside metallization was applied.

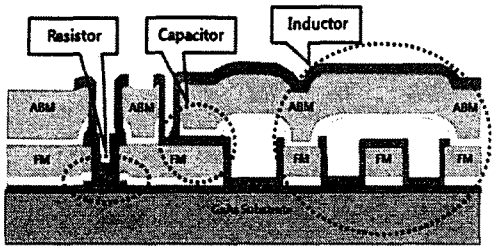

Fig.1 Cross-sectional view of the GaAs integrated passive device

3. Design and Layout

The final equivalent circuit of power divider is shown in Fig.2. When the operating frequencies are set at f_1 = 900 MHz and f_2 = 1800 MHz, the design parameters are $C_1 = C_3 = 2.5$ pF, $C_2 = 1.25$ pF, $L_1 = L_3 = 6.25$ nH, and $L_2 = 12.5$ nH. The element values can be calculated by the equations (1), (2), and (3) [3].

$$C_1 = C_3 = \frac{1}{\omega_0 z_0}, \quad C_2 = \frac{1}{2\omega_0 z_0} \tag{1}$$

$$L_1 = L_3 = \frac{z_0}{\omega_0}, \quad L_2 = \frac{2z_0}{\omega_0} \tag{2}$$

$$f_0 = \sqrt{f_1 \times f_2} \tag{3}$$

Where ω_0 is notch frequency and Z_0 is load impedance. The simulation was done with Agilent's ADS 2008.

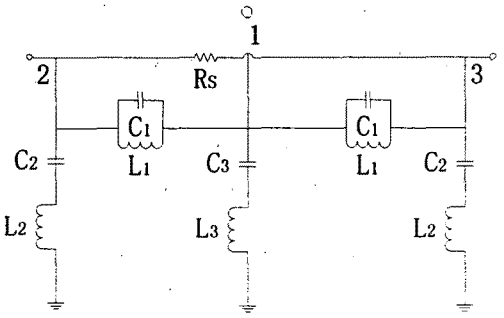

Fig.2 The final equivalent circuit of power divider

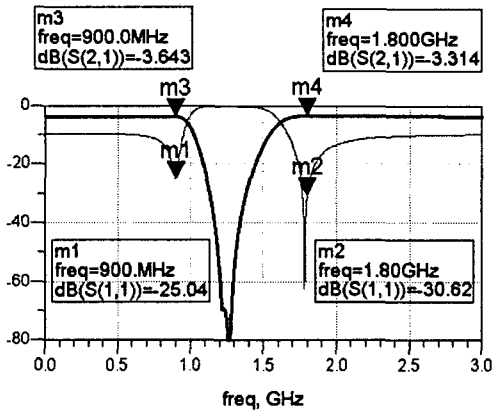

Fig.3 The insertion loss and return loss of the dual band power divider

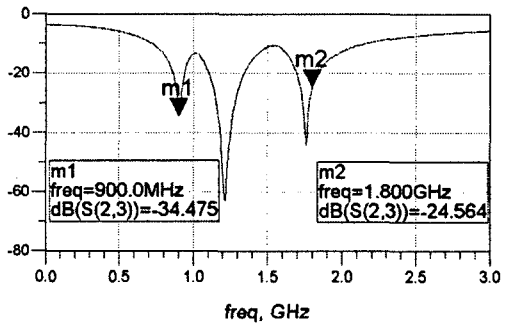

Fig.4 The isolation of the dual band power divider

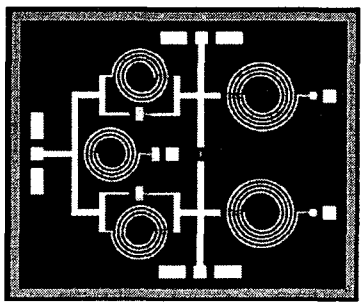

Fig. 5 Layout of the designed dual-band power divider

4. Conclusion

We realized a small size and low cost dual band power divider IC chip using IPD processes for 900/1800 MHz, and it was possible to provide both good matching and isolation at any two arbitrary frequencies where needed. The simulation results of power divider were shown in Fig.3 and Fig.4; isolation of more than -24 dB, insertion loss of nearly -3.5 dB, and return loss of about -25 dB. The circuit layout was shown in Fig.5, and the size is 2.5×2 mm^2. It was fabricated using the aforementioned IPD technology on a SI-GaAs wafer. Using the IPD process we can obtain an IC chip with very small size and low cost.

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