고성능 PMOSFET을 위한 Ni-silicide와 p+ source/drain 사이의 barrier height 감소

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Reduction of Barrier Height between Ni-silicide and p+ source/drain for High Performance PMOSFET

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Abstract : As the minimum feature size of semiconductor devices scales down to nano-scale regime, ultra shallow junction is highly necessary to suppress short channel effect. At the same time, Ni-silicide has attracted a lot of attention because silicide can improve device performance by reducing the parasitic resistance of source/drain region. Recently, further improvement of device performance by reducing silicide to source/drain region or tuning the work function of silicide closer to the band edge has been studied extensively. Rare earth elements, such as Er and Yb, and Pd or Pt elements are interesting for n-type and p-type devices, respectively, because work function of those materials is closer to the conduction and valance band, respectively.

In this paper, we increased the work function between Ni-silicide and source/drain by using Pd stacked structure (Pd/Ni/TiN) for high performance PMOSFET. We demonstrated that it is possible to control the barrier height of Ni-silicide by adjusting the thickness of Pd layer. Therefore, the Ni-silicide using the Pd stacked structure could be applied for high performance PMOSFET.

Key Words : Ni-silicide, Pd stacked structure, barrier height, high performance PMOSFET

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