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전류연속모드 승압형 컨버터의 효율 분석에 관한 연구

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A Study on the efficiency analysis of CCM boost converter

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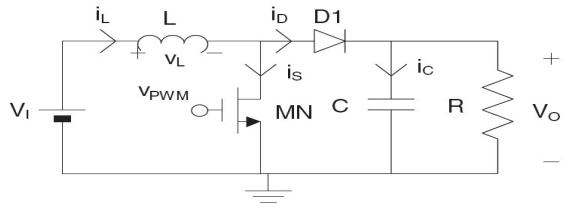
Abstract - This paper presents the efficiency analysis of CCM(Continuous Current Mode) boost converter. A thorough efficiency analysis of a boost converter taking into account the conduction losses, the diode power loss, the switching losses, the gate-drive loss and the capacitive switching loss, for both continuous conduction mode is presented.

1. INTRODUCTION

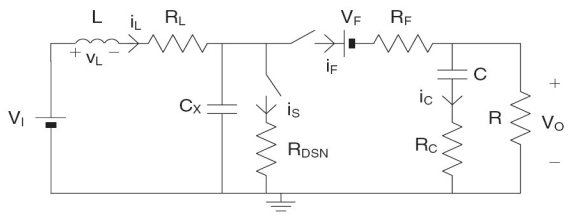
The boost converters are widely used to obtain a voltage higher than the battery source one. During the design step, the efficiency of such a converter can be accurately predicted only if the main dissipation sources are considered. In this paper a thorough efficiency analysis of boost PWM converter is carried out. In particular, relationships that take into account the conduction losses, the diode power loss, the switching losses, the gate-drive loss, and the capacitive switching loss both for CCM are given. The expressions developed can be effectively used to predict the converter circuit behaviour both for a constant input voltage and output voltage operation, and can help the designer to improve the converter performance.

2. ANALYSIS OF BOOST CONVERTER

The conventional schematic of a boost converter is shown in Figure 1. It consists of an inductor, L, a power transistor MN, which implements a controllable switch, a diode, D1, a filter capacitor, C, and a load resistance, R.

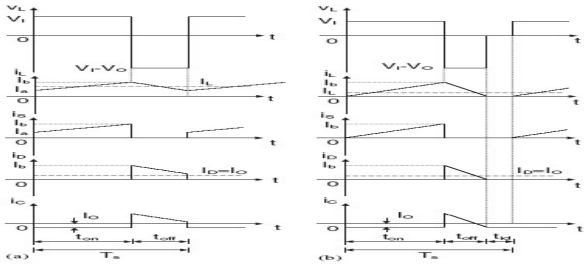


<Fig. 1> Boost converter.



<Fig. 2> Boost converter equivalent circuit including the parasitic components

The equivalent circuit of the boost converter taking into account the parasitic components is shown in Figure 2, where capacitor, C_X is the equivalent parasitic capacitance at the drain of transistor MN, and the other components were defined above. Assuming the transistor-switch is turned on and off at the constant switching frequency, $f_S = 1/T_S$, the inductor voltage and the current waveforms of the converter operated at CCM and DCM are depicted in Figures 3(a) and (b), respectively.



<Fig. 3> Boost PWM converter waveforms
(a) CCM (b) DCM

2.1. CCM Boost Converter Analysis

Assume the boost converter to work in CCM. As far as the conduction loss in the inductor is concerned, we have

$$P_{RL} = R_L \times I_{L,RMS}^2 \tag{1}$$

From Figure 3(a), the root mean squared current through the inductor, $I_{L,RMS}$ can be evaluated as follows:

$$I_{L,RMS} = \left[\frac{1}{T_S} \int_0^{T_S} i_L^2(t)\, dt \right]^{1/2} = \left\{ \frac{1}{T_S} \int_0^{t_{ON}} \left(I_a + \frac{\Delta I_L}{t_{ON}} t \right)^2 dt + \frac{1}{T_S} \int_{t_{ON}}^{T_S} \left(I_a + \Delta I_L \frac{T_S - t}{T_S - t_{ON}} \right)^2 dt \right\}^{1/2} \tag{2}$$

Since the minimum inductor current, I_a is equal to $I_L - \Delta I_L/2$ solving (2) we have

$$I_{L,RMS} = \left[(M I_O)^2 + \frac{\Delta I_L^2}{12} \right]^{1/2} \tag{3}$$

being M the ratio between the dc output voltage V_O and the input voltage V_I, current I_O the dc output current through the load resistance R (i.e. V_O/R) and ΔI_L the ripple of the inductor current, given by

$$\Delta I_L = \frac{V_O}{L f_S} \frac{M-1}{M^2} \tag{4}$$

The diode power loss is

$$P_D = V_F I_D + R_F I_{D,RMS}^2 = V_F I_O + \frac{R_F}{M} I_{L,RMS}^2 \tag{5}$$

The power loss in the ESR, R_C results

$$P_{RC} = R_C I_{C,RMS}^2 = \frac{R_F}{M} I_{L,RMS}^2 - R_C I_O^2 \tag{6}$$

Observing the power transistor current behaviour, it is apparent that its averaged value, I_S, as well as its root mean squared, $I_{S,RMS}$ are given by

$$I_S = \frac{t_{on}}{T_S} \frac{(I_a + I_b)}{2} = D I_L = (M-1) I_O \tag{7}$$

$$I_{S,RMS} = \left[\frac{1}{T_S} \int_0^{T_S} i^2_S(t)\, dt \right]^{1/2} = \left[D \frac{(I^2_a + I^2_b + I_a I_b)}{3} \right]^{1/2} = \left(\frac{M-1}{3} \right)^{1/2} I_{L,RMS} \quad (8)$$

The power loss in the transistor-switch MN depends on four dissipation sources. Specifically, the first cause is the conduction loss, P_S in the resistance R_{DSN} which, taking into account the relationship (8) can be evaluated as follow

$$P_S = R_{DS}\, I^2_{S,RMS} = R_{DSN} \frac{M-1}{M}\, I^2_{L,RMS} \quad (9)$$

The second dissipation source is the switching loss P_{SW} due to turn-on and turn-off of power transistor and it is given by

$$P_{SW} = \frac{1}{2} (V_O + V_F) \left(M I_O + \frac{\Delta I_L}{2} \right) (t_{rv} + t_{fi})\, f_S \quad (10)$$

where t_{rv} and t_{fi} are the rise and the fall times of drain-source voltage and drain current, respectively. Note that, in determining Equation (10) we have assumed some reasonable approximations. Specifically, since the current at turn-on of transistor switch is smaller than the turn-off one, only power loss on the turn-off can be considered.

The third contribution is the gate-drive loss P_G, due to raising and lowering the power transistor gate, which results

$$P_G = C_{GN}\, V^2_O\, f_S \quad (11)$$

being C_{GN} the equivalent capacitance at the gate of power transistor MN. It is worth noting that to obtain relationship (11) the power supply of the control circuit has been assumed equal to the output voltage. Finally, the last contribution is the capacitive switching loss P_X due to the equivalent parasitic capacitance C_X, which is given by

$$P_X = C_X\, V^2_O\, f_S \quad (12)$$

Collecting the terms in Equations (1)-(12), the efficiency of the PWM boost converter results

$$\eta_{CCM} = \frac{P_O}{P_O + P_{RL} + P_D + P_{RC} + P_S + P_{SW} + P_D} = \left\{ 1 + \frac{V_F}{V_O} + \frac{R_Y I_O}{V_O} + \frac{R_Z}{V_O I_O} \cdot \frac{\Delta I^2_L}{12} + \left[\frac{1}{2} \left(1 + \frac{V_F}{V_O} \right) \cdot \left(M + \frac{\Delta I_L}{2 I_O} \right) \cdot (t_{rv} + t_{fi}) + \frac{V_O}{I_O} (C_{GN} + C_X) \right] f_S \right\}^{-1} \quad (13)$$

where R_Y and R_Z are defined as

$$R_Y = R_L M^2 + R_F M + (R_C + R_{DSN} M) \cdot (M-1) \quad (14)$$

$$R_Z = R_L + R_{DSN} \frac{(M-1)}{M} + \frac{R_F + R_C}{M} \quad (15)$$

From relationship (13) it is possible to predict the converter efficiency taking into account all the dissipation sources. Moreover, if the switching frequency f_S is low enough so that the switching losses can be neglected, expression (13) can be rewritten neglecting the term in square bracket and, hence, substituting (14)-(15) an approximate efficiency, $\eta_{CCM,A}$ can be evaluated as

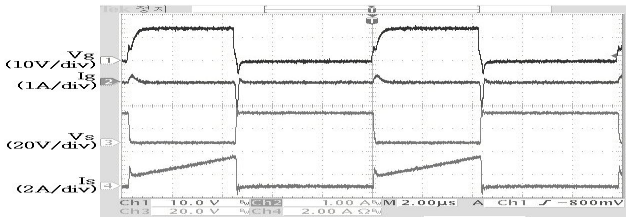
$$\eta_{CCM,A} = \left\{ 1 + \frac{V_F}{V_O} - R_C \frac{I_O}{V_O} + \frac{I_O}{V_O} \left[R_L + R_{DSN} + \frac{V_I}{V_O} (R_F + R_C - R_{DSN}) \right] \times \left[\left(\frac{V_O}{V_I} \right)^2 + \frac{(V_O - V_I)^2\, V^2_I}{12 (L f_S I_O V_O)^2} \right] \right\}^{-1}$$

2.2 Experimental Result and Efficiency Analysis

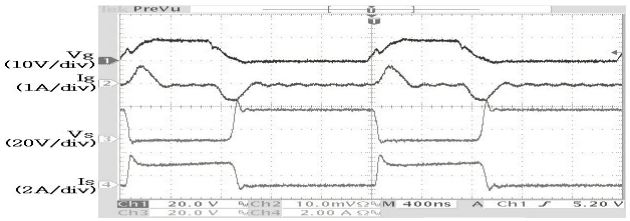
The prototype of Boos converter has been implemented to verify the loss analysis. Table. 1 shows specifications and parameters about the prototype.

<Table. 1> The specifications and parameters used in converter

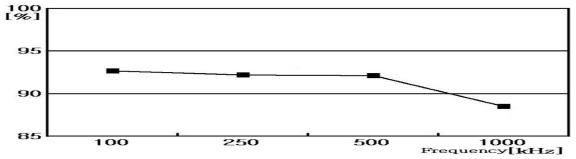
Input voltage (V_I)	DC 15 V
Output voltage (V_O)	DC 24 V
Output power (P_O)	24 W
Boost inductor (L)	38.57 μH. TDK
Power transistor (MN)	ISFS530A. Fairchild
Diode (D_1)	SB340. Fairchild
filter capacitor (C)	1000 μF



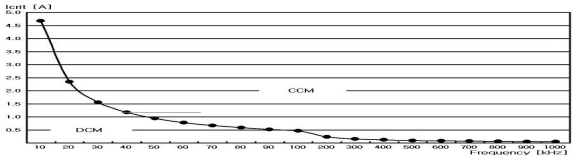
<Fig. 4> Gate voltage, gate current, switch voltage, and switch current of boost converter (100kHz full load)



<Fig. 5> Gate voltage, gate current, switch voltage, and switch current of boost converter (500kHz full load)



<Fig. 6> The experiment result of efficiency



<Fig. 7> The critical-current variation according to frequency(theoretical data) (Vi = 15[V], L = 38.57[uH], R = 24[Ω])

3. CONCLUSIONS

In this paper, a detailed efficiency analysis of a boost dc-dc PWM converter, taking into account all the chief sources of dissipation, for CCM was carried out. The proposed expressions agree very well with simulated ones, and, therefore, can help the designer for designing a PWM converter operated with the highest efficiency for a given application.

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