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# Dry etching of SiC in inductively coupled $SF_6/O_2$ Plasma

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A buried gate structure was suggested to reduce trapping induced instabilities and to obtain higher output power density in SiC MESFETs. Thicker channel allows for higher drain saturation current and thinner channel below the gate ensures the effective control of channel by the gate bias. Conventional 4H-SiC planar MESFETs were fabricated without a channel recess etching process to prevent the damage from the bombardment of energetic ions. In a buried-gate planar MESFET structure, only gate regions are defined using dry etching, and other channel regions are free of damage. But dry etch process makes the gate Schottky contacts have higher leakage current and lower breakdown voltages. To optimize the buried gate etching process, the effect of dry etch induced damage on SiC surfaces has been investigated using Ni Schottky diodes.

To obtain low leakage current, Ni Schottky diodes were fabricated on the SiC substrates which were inductively coupled plasma (ICP) etched at different conditions using a mixture of $SF_6$ and $O_2$. The increase of etch rate at higher bias power is due to the increase in the energy of ion bombardment which will enhance the physical sputtering and chemical reaction of the surface. This damage may induce defects like dislocations, vacancies. I-V characteristics of fabricated diodes were measured using HP4155A. The barrier height($\Phi_B$) and ideality factor(n) were obtained from forward I-V measurements by fitting standard thermionic theory. As the bias power increases, the barrier height was observed to decrease and the ideality facter inecreased tending to the non-ideal behaviour. Low bias power ICP could reduce the reverse leakage current at 100 V to $3x10^{-5}$ A/cm$^2$.