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Development of RSFQ Logic Circuits and Delay Time Considerations in Circuit Design

J. H. Kang [a] and J. Y. Kim [b]

[a] *University of Incheon, Incheon, S. Korea*

[b] *Kiscom Inc., Seoul, S. Korea*

RSFQ logic circuits are very fast and consume very low power. Therefore, RSFQ logic circuit is a very good candidate for future electronic devices. Successful developments of various RSFQ logic circuits, including a digital-to-analog converter, an analog-to-digital converter, a switching device, a router, and a voltage standard have been reported. Also, a toggle flip-flop (TFF) circuit was built with this technology and was operated at 770 GHz. The focus of the RSFQ circuit development has been on the advancement of analog-to-digital converters and microprocessors. Recent works on RSFQ ALU development showed the successful operation of an 1-bit block of ALU at 40 GHz. The study of an RSFQ analog-to-digital converter has been extended to the development of a single chip RF digital receiver.

Compared to the voltage logic circuits, RSFQ circuits operate based on pulse logic. This naturally leads the circuit structure of RSFQ circuit to be pipelined as shown for the 4-bit ALU block diagram in the Figure. Delay time on each pipelined stage determines the ultimate operating speed of the circuit.

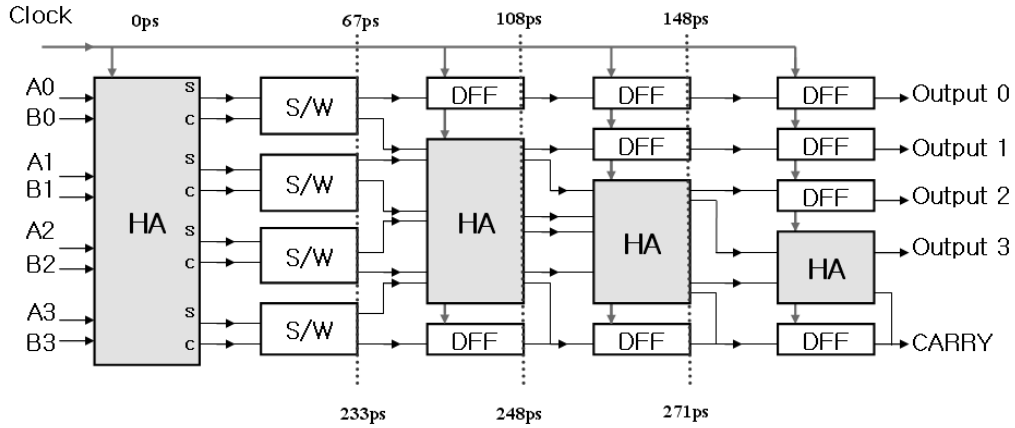

Figure. Block diagram of the 4-bit ALU.

The problem of fluctuation-induced digital errors in a rapid single flux quantum (RSFQ) circuit is also very important issue. The bit error rate of an RSFQ switch used in superconductive Arithmetic Logic Unit should

have a very low error rate in the optimal bias. Theoretical estimates of the RSFQ error rate are of order 10^{-50} per bit operation. In experiment, the bit error rate of 2.18×10^{-12} was measured when the bias to the RSFQ switch was 0.398mA that was quite off from the optimum bias of 0.6mA.

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