A 1.2-V 0.18-μm Sigma-Delta A/D Converter

for 3G wireless Applications

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Abstract

A low-voltage switched-capacitor 2nd-order ΣΔ modulator using full feed-forward is introduced. It has two advantages: the unity signal transfer function and reduced signal swings inside the ΣΔ loop. These features greatly relax the DC gain and output swing requirements for Op-Amp in the low-voltage ΣΔ modulator. Implemented by a 0.18-μm CMOS technology, the ΣΔ modulator satisfies performance requirements for WCDMA and CDMA2000 standards.

I. Introduction

The development of broadband communications systems is stimulating the demand for high-resolution (>11 bits) analog-to-digital converters (ADCs) for signal bandwidth of several megahertz (>2 MHz). However, the aggressive scaling of advanced CMOS VLSI technologies makes it hard to design wide dynamic range ADCs because of limited signal range. Also, increased power consumption is needed to attain wide dynamic range ADCs with low supply voltage. This paper explores the means to deal with these challenges in the design of sigma-delta A/D converter.

II. Low-Voltage ΣΔ Modulator

Fig.1 shows the conventional architecture of a 2nd-order sigma-delta (ΣΔ) modulator. The z-domain transfer functions of this ΣΔ modulator are

\[ Y = z^{-2} \cdot X + Q \cdot (1 - z^{-1})^2 \]  
\[ U_i = (1 - z^{-2}) \cdot X - Q \cdot (1 - z^{-1})^2 \]  
\[ V_i = \frac{z^{-1}}{1-z^{-1}} \cdot X - z^{-1} \cdot (1 - z^{-1}) \cdot Q \]  
\[ U_2 = z^{-1} \cdot X - Q \cdot (1 - z^{-1})^2 - Q \cdot (1 - z^{-1}) \]  
\[ V_2 = z^{-2} \cdot X + Q \cdot (-2 \cdot z^{-1} + z^{-2}) \]  
\[ W_i = X + Q \cdot (-2 \cdot z^{-1} + z^{-2}) \]

From the transfer functions of two ΣΔ modulator architectures shown above, it can be observed that RISR (Fig.2) architecture not only reduces integrator swing range considerably [1]. The z-domain transfer functions for this ΣΔ modulator (Fig.2) are

\[ Y = X + Q \cdot (1 - z^{-1})^2 \]  
\[ U_i = -Q \cdot (1 - z^{-1})^2 \]  
\[ V_i = -z^{-1} \cdot (1 - z^{-1}) \cdot Q \]  
\[ V_2 = -z^{-2} \cdot Q \]  
\[ W_i = X + Q \cdot (-2 \cdot z^{-1} + z^{-2}) \]

Fig.2 shows the 2nd-order ΣΔ modulator architecture which reduces integrator swing range considerably [1]. The z-domain transfer functions for this ΣΔ modulator (Fig.2) are

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\[ V_2 = -z^{-2} \cdot Q \]  
\[ W_i = X + Q \cdot (-2 \cdot z^{-1} + z^{-2}) \]

From the transfer functions of two ΣΔ modulator architectures shown above, it can be observed that RISR (Fig.2) architecture not only reduces the signal range of integrators extensively but also makes the input not pass through the integrators. These features alleviate the op-amp performance requirements considerably such as slew-rate, DC-gain linearity, and output swing range. Therefore, the RISR ΣΔ modulator architecture is a proper one for low-voltage and low-power applications.
III. Implementations

The dynamic range requirements of the ΣΔ modulator are calculated to be above 70dB for 1.92MHz (WCDMA) and 80dB for 614kHz (CDMA2000) bandwidth. Extensive behavioral simulations using MATLAB show that 2nd-order RISR ΣΔ modulator with 3-bit ADC is appropriate [2]. Fig. 3 shows the single ended schematic of the ΣΔ modulator although actual implementation is fully-differential. Behavioral simulations show that DC gain of 45dB, GBW of 400 MHz, and ±0.4V output swing are required for the 1st op-amp. 2nd op-amp is needed to satisfy GBW of 200 MHz with the same DC gain and output swing requirement.

1st and 2nd Op-amps are implemented using pMOS input folded-cascode architecture and satisfy all the performance requirements explained above with 1mW and 0.5mW power consumption, respectively. Because of low-supply voltage (1.2V), input common-mode (CM) and output common-mode voltage are made differently; input CM voltage is 0.3V and output CM voltage is 0.6V. Considering dynamic range requirement (above 70dB for 1.92MHz bandwidth), the size of sampling capacitors are calculated as Cs1 of above 100fF and Cs2 of above 30fF. When actually implementing, Cs1 of 700fF and Cs2 of 400fF are used because Cs1 consists of 7 unit capacitors of 100fF. As shown in the Fig. 2 and Fig. 3, the RISR architecture needs adding operation of input and both outputs of integrators. This is realized using sampling capacitors network shown in the Fig. 4 [3]. The capacitors also cancel offset of comparator.

IV. Simulation Results & Conclusions

Fig. 5 shows the transient simulation results when applying input of -6dBFS (VREF_P=1.2V) amplitude and 200 kHz frequency. Fig. 6 shows FFT result for the transient response. SNDR is 60dB when clock frequency is 76.8MHz; oversampling ratio is 20 for 1.92MHz bandwidth. Total power consumption is 15mW. The 3-bit DAC employs data-weighted averaging (DWA) to linearize the DAC output.

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References