제안된 DC offset 상쇄 회로를 이용한 저전력의 프로그래머블 이득 증폭기

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A Low-Power Programmable Gain Amplifier utilizing Proposed DC offset Cancellation Resistors

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Abstract

Ultra wideband communications using impulse signal is recently one of the key technologies for wireless communications due to its feasibility to various applications. Ultra wideband (UWB) RF chaotic system, a modified UWB system, using noise-like signal has advantageous features including low power consumption, efficient power management, compactness, and robustness in multi-path and thus lower price. Since UWB RF chaotic transceiver basically composed entirely of single ended output building block, operational amplifiers should be inverting or non-inverting. In this paper, a programmable gain amplifier (PGA) was implemented by using a proposed simple DC offset voltage cancellation circuit, only for inverting or non-inverting operational amplifiers, and a 0.18μm CMOS technology. The DC offset voltage cancellation circuit, a resistor, overcomes the classical DC offset problems that degrade the sensitivity performance of direct chaotic transceivers. The voltage gain is varied by digitally controlling the input switched resistors and the overall PGA gain varies from 22dB to 30dB with 1dB per step. With a 0.18μm CMOS technology, this work dissipates 0.81mW from a 1.8V supply voltage.

1. INTRODUCTION

The breakthrough of wireless communication in recent years has created a demand for smaller and cheaper portable handsets. Much effort has been made to fulfill these requirements, often with success [1]. The era of portable personal communication systems is expanding in an unprecedented fashion and rapidly becoming a part of daily lives. The highly integrated single chip transceiver is developed to reduce cost, power consumption and size. Comparing the existing architecture, chaotic RF transceiver architecture shows satisfaction for all of these demands including highly integrality, lower price.

Programmable gain amplifier (PGA) is one of the essential components for chaotic systems as shown in Fig. 1. To increase the dynamic range of the receivers a PGA is added to overcome the change in input signal strength by producing a known output voltage. As direct conversion receiver (DCR) has a lot of well known problems [2], i.e. DC offsets and flicker noise. These problems pose new challenges to design a PGA for the DCR. It should have fast lock time with wide gain tuning range and most importantly it should be equipped with automatic DC offset cancellation [4].

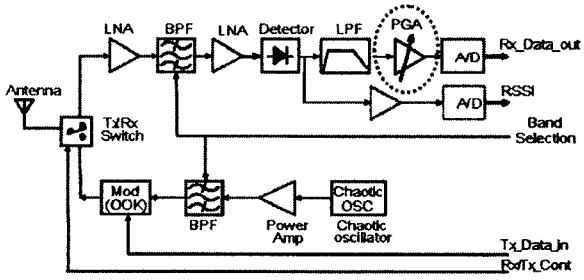

Fig. 1. Block diagram for chaotic transceiver

DC offset will degrade the receiver dynamic range. AC coupling of each stage is the easier way to remove the offset. However, this approach requires large capacitor values that are not realizable on-chip. The other method is detected and removed by digital time-averaging or by using more complex digital algorithm. This sort of digital cancellation requires the analog baseband circuits to have enough spurious-free dynamic range (SFDR) to overcome the DC offset [3].