A CMOS VLSI Integrated RF Transceiver System for Wireless Sensor Networks in Sub-GHz

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Abstract

A fully CMOS integrated radio frequency (RF) transceiver for wireless sensor networks in sub-GHz ISM-band applications is implemented and measured. The IC is fabricated in 0.18-㎛ CMOS technology and packaged in LPCC package. The fully monolithic transceiver consists of a receiver, a transmitter and a RF synthesizer with on-chip VCO. The chip fully complies with the IEEE 802.15.4 WPAN standard in sub-GHz mode. The receiver sensitivity is –98dBm and the transmitter achieves less than 6.3% error vector magnitude (EVM) for 40kbps mode. The chip uses 1.8V power supply and the current consumption is 14mA for reception mode ad 16mA for transmission mode.

I. Introduction

Recently, the desire for wireless connectivity has led an exponential growth in wireless communication. In particular, wireless sensor networks are potential wireless network application for the following future ubiquitous computing system. Wireless sensor networks are an emerging research area with potential applications in environmental monitoring, surveillance, military, health and security [1]. The power dissipation of wireless sensor networks does require low power consumption for several years' operation.

There has been a great deal of interest in realizing low power, low cost, compact RF transceiver for wireless sensor networks. Several technological trends that are driving the technical evolution of wireless technology include the process scaling of CMOS transistors and higher and higher bandwidth available at ISM bands. Almost all of the license free bands propose both linear and nonlinear modulation standards for wireless applications, thus requiring different design optimizations in the RF transceiver. Along with these issues, there exists the challenge to develop fully integrated wireless solutions in silicon-based substrates [2].

In this paper we present the development of a fully single chip 0.18-㎛ CMOS RF transceiver targeted towards ubiquitous wireless sensor networks in sub-GHz ISM-band applications.

Section 2 of this paper describes the architecture and implementation of RF transceiver. The measurement results are presented in Section 3, then some final conclusions are offered in Section 4.

II. RF SYSTEM IMPLEMENTATION

A. RF transceiver architecture

The communication nodes are required to integrate with one die for low power and low cost wireless sensor network applications. With first step, we did implement RF transceiver chip including an ADC and a DAC. Fig.1 shows the architecture of a radio chip, which consists of a receiver, a transmitter, and a frequency synthesizer with on-chip VCO. The receiver adopts zero-IF architecture [3], [4] to have low power consumption, low cost and small size. The sub-GHz RF signal is first amplified by a low noise amplifier (LNA) and then down-converted to zero-IF I/Q signals by two identical mixers driven

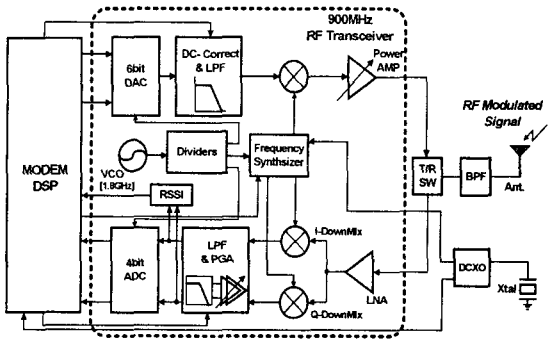

Fig.1 RF transceiver block diagram supporting wireless sensor networks in sub-GHz ISM-band

by quadrature local-oscillator (LO) signals from a frequency synthesizer. At the analog baseband stage, using a third-order RC filter and programmable gain amplifier simultaneously performs channel selection filtering, signal amplification, and dc-offset cancellation. And I/Q 4bit dual flash-ADCs are connected for interface of MODEM block.

The transmitter adopts a general zero-IF modulation with up-conversion mixer. Baseband BPSK signals generated by digital modulator in MODEM block are followed a 6-bit DAC. A mixer up-converts the baseband signal directly 900-MHz, which is combined by RC low-pass filter. Since BPSK modulation is a constant envelop modulation, a nonlinear power amplifier with high efficiency can be used.

For generating 900-MHz LO signals with 2-MHz channel spacing, an integer-N frequency synthesizer derived from a 30-MHz crystal oscillator with 30ppm accuracy is implemented. A 1.8GHz LO signal is generated by a voltage-controlled oscillator (VCO) with a small area and high Q on-chip inductor. The 900-MHz LO I/Q signals are then generated by a divide-by-two circuit. The frequency synthesizer is implemented in fully differential type, for immunity to common mode noise.

B. RF transceiver design

RF transceiver is designed using 0.18-㎛ CMOS process including six metal layers with 2-um thick top