개인무선통신을 위한 다이렉 컨버젼 수신기의 CMOS 아날로그 프런트엔드 회로설계

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Design of a CMOS Analog Front End for a WPAN Receiver

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Abstract

This paper describes a low-voltage and low-power channel selection analog front end with continuous-time low pass filters and highly linear programmable-gain amplifier(PGA). The filters were realized as balanced Gm-C biquadratic filters to achieve a low current consumption. High linearity and a constant wide bandwidth are achieved by using a new transconductance(Gm) cell. The PGA has a voltage gain varying from 0 to 65dB, while maintaining a constant bandwidth. A filter tuning circuit that requires an accurate time base but no external components is presented. With a 1-Vrms differential input and output, the filter achieves -85dB THD and a 78dB signal-to-noise ratio. Both the filter and PGA were implemented in a 0.18um 1P6M n-well CMOS process. They consume 3.2mW from a 1.8V power supply and occupy an area of 0.19mm^2.

Index terms ? Channel selection filters, DC offset, programmable gain amplifier, tuning circuit

I. Introduction

The demand for low-cost, low-power wireless tranceivers operating in the Wireless Personal Area Network(WPAN) has led to extensive research on RF circuit design[1][2]. Particularly, since one of the characteristics of such a WPAN transceiver is that it has a wider channel spacing than the bandwith of a channel has[3], its filter attenuation requirement is lower than other wireless communication specifications[4][5][6][7]. Thus, it is possible to use a filter of a lower order, and this will lead to a lower power dissipation and cost. This paper suggests that the Analog Front End in transceiver is relevant to this WPAN.

II. Analog Front End Design

Figure 1 shows the Analog Front End (AFE) of a realized WPAN receiver. The third order Butterworth filter was implemented cascading a biquad cell and a single pole cell, and the programmable gain cell was stationed at the middle to improve the cascaded dynamic range. The AFE design is concentrated on optimizing the dynamic range and keeping the required die area small and low power consumption. The baseband noise is dominated by the thermal noise of the PMOS current sources at the Mixer output. The flicker noise is not a significant problem at baseband since all transistors are designed for a long channel length for better matching. And the output of the DAC is DC blocked using a Modem control signal to minimize the effect of the internal DC offsets from limiting the dynamic range of the receiver.

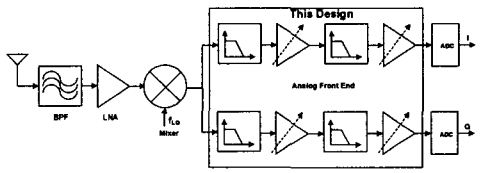

Fig. 1. Block diagram of the analog front end

2.1 Channel Selection Filter

The Channel filter allows a signal of the desired band to pass, and attenuates the adjacent channel and the alternate channel. The filter requirement in this paper is as follows. Since it is a DCR structure, 1/f noise should be reduced and the DC offset should be small. And in order to alleviate the SFDR requirements of the PGA and the ADC, most of the interference is filtered in the