플라즈마 디스플레이 패널을 위한 단일 소프트-스위칭 다단계 에너지 회수 회로 드라이버

하꼬보 아기용, *문건우

Single Soft-Switching Multi-Level Energy Recovery Circuit Driver for Plasma Display Panel

Jacobo Aguillón-García, *Gun-Woo Moon
Department of Electrical Engineering and Computer Science,
Korea Advanced Institute of Science and Technology,
*E-mail: gwmoon@ee.kaist.ac.kr

ABSTRACT

The power source of an AC-PDP for sustainer circuit is operated in high-voltage and high frequency switching during the process required to achieve the gas discharge current to generate light in a PDP panel. Since PDP has the characteristics of a pure capacitive load, the displacement current that occurs during charge and discharge generates considerable reactive power. An auxiliary circuitry called Energy Recovery Circuit (ERC) reduces the capacitive displacement current. However, this auxiliary topology also bears high stress in its components. In this paper, a multilevel voltage wave shaping sustainer circuit with auxiliary ERC characteristics for an AC-PDP driver is proposed. A comparative analysis and experimental results are presented.

1. INTRODUCTION

The plasma display panel (PDP), has many desirable advantages over other competing flat panel displays and is expected to be the most promising flat panel display of the next generation [1, 2]. Due to the construction of the PDP, a dielectric layer exist between surface discharging electrodes and also between opposed discharging electrodes, therefore a intrinsic capacitance C_P exist [3-5]. Thus, when applying a sustain pulse on the electrodes for charging and discharging the inter-electrode capacitor, the energy supplied from a power source is: $P = C_P V_S^2$, where C_P is the equivalent panel capacitance and V_S is the source voltage.

The common architecture used as sustainer driver circuit is based on a full-bridge inverter configuration and is implemented by Y and X driver board type [1]. As the PDP has the characteristics of a pure capacitive load, the displacement current that occurs during charging and discharging the PDP panel causes a considerable energy loss [1-5]. Furthermore, this surge current will give rise to EMI noises and increase the surge current ratings of power switches. If an inductor is placed in series with the panel, then C_P can be charged and discharged through the inductor. This type of circuits is often called energy-recovery circuit (ERC). The main characteristic of the topologies classified as multilevel, is the use of commutation devices connected in series, allowing the distribution of the voltage and reducing stress in the commutation switches, so the use of less expensive components is feasible [6-8]. The proposed circuit features less device elements, voltage stresses and significantly reduced rms current stresses, compared with those of the conventional and multilevel ones.

2. OPERATIONAL PRINCIPLES

The common driving scheme for a plasma display panel (PDP) is the address-display-separation (ADS) method [9, 10]. The address period consists of a reset and address setup. The rest is the display period where the sustaining action is achieved. The proposed single driver and ERC in this article are based on Weber and Wood architecture [3-5]. Topology and key waveforms are shown in figure 1(a-b), respectively. For the analysis of the sustaining circuit operation, the following assumptions are made:

- The voltage of the input capacitors is considered as constant voltage $V_S/4$.
- The input capacitor values are equal; $C_1 = C_2 = C_3 = C_4 = C$.
- The input capacitance is much larger than the panel capacitance; $C_P << C$.
- The switches S_1, S_2, S_{M1} and S_{M2} are considered ideal except for $R_{ds\text{-}on}$.
-

Figure 2 shows the operational modes and the current path for each case of the proposed circuit.

Mode 1 ($t_0<t<t_1$) Precharge Mode: Switch S_{1a} is closed and therefore the energy stored in C_3 and L_{ERC} is transferred to C_P via path C_3-S_{1a}-D_{1b}-L_{ERC}-C_P in a resonant mode. Then, the current through L_{ERC} and voltage panel C_P are:

$$I_{L_{ERC}}(t) = \frac{V_S}{4} \cdot \frac{1}{Z_r\sqrt{1-\zeta^2}} \cdot e^{-\zeta(t-t_0)} \cdot \sin\left[\omega_d (t-t_0)\right], \quad (1)$$

$$V_{C_P}(t) = \frac{V_S}{4}\left(1 - e^{-\zeta\omega_n(t-t_0)} \cdot \left(\cos(\omega_d(t-t_0)) + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left[\omega_d (t-t_0)\right]\right)\right).$$

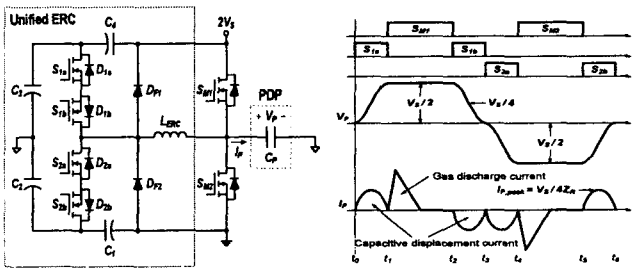
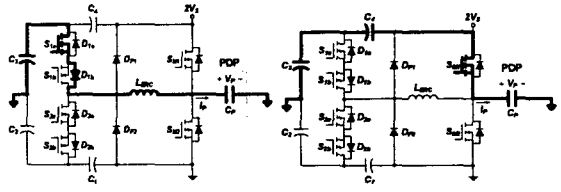


Fig. 1 Schematic diagram and key waveforms of proposed circuit.



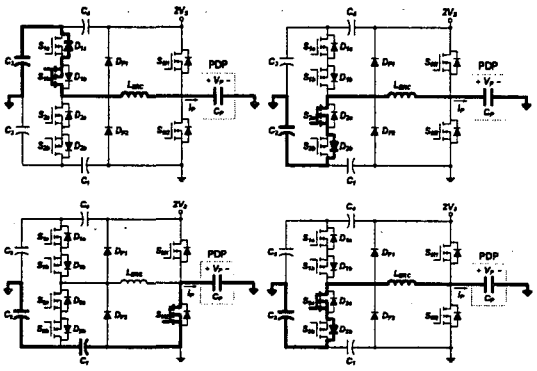


Fig. 2 Operational modes of the proposed circuit.

where,

$$\omega_r = \omega_r\sqrt{1-\zeta^2},\ \zeta = {R_{eq}}/{Z_r},\ R_{eq} = R_{ds\_S} + R_D \text{ and } Z_r = \sqrt{{L_{ERC}}/{C_P}}.$$

Note that $R_{ds\text{-}S}$ is the channel resistance of switch and R_D is diode's forward voltage.

Mode 2 (t_1<t<t_2) Gas-discharge Mode: Switch S_{M1} transfers the energy in C_3+C_4 to C_P via path C_3-C_4-S_{M1}-C_P. If the peak voltage reached in C_P in previous stage is:

$$V_{C_{P\_peak}} = \frac{V_S}{4}\left(1 + \frac{e^{-\pi\zeta}}{\sqrt{1-\zeta^2}}\right). \tag{2}$$

Then, the difference between the peak voltage during t_0<t<t_1 and the voltage in t_1<t<t_2 is as follows:

$$\Delta V = {V_S}/{2} - V_{C_{P_{peak}}} = \frac{V_S}{4} - \frac{V_S \cdot e^{-\pi\zeta}}{4\sqrt{1-\zeta^2}}. \tag{3}$$

Mode 3 (t_2<t<t_3) Predischarge Mode: Switch S_{1b} is closed and therefore the energy stored in C_3 and L_{ERC} is transferred to C_P via path C_P-L_{ERC}-S_{1b}-D_{1a}-C_3 in a resonant mode. Then, the current trough L_{ERC} and voltage panel C_P are:

$$I_{L_{ERC}}(t) = -\frac{V_S}{4}\cdot\frac{1}{Z_r\sqrt{1-\zeta^2}}\cdot e^{-\zeta(t-t_2)}\cdot\sin\left[\omega_d(t-t_2)\right], \tag{4}$$

$$V_{C_P}(t) = \frac{V_S}{4}\left(1 + e^{-\zeta\omega_n(t-t_2)}\cdot\left(\cos(\omega_d(t-t_2)) + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left[\omega_d(t-t_2)\right]\right)\right).$$

Mode 4 (t_3<t<t_4) Precharge Mode: Switch S_{2a} is closed and therefore the energy stored in C_2 and L_{ERC} is transferred to C_P via path L_{ERC}-S_{2a}-D_{2b}-C_2-C_P in a resonant mode. Then, the current trough L_{ERC} and voltage panel C_P are:

$$I_{L_{ERC}}(t) = -\frac{V_S}{4}\cdot\frac{1}{Z_r\sqrt{1-\zeta^2}}\cdot e^{-\zeta(t-t_3)}\cdot\sin\left[\omega_d(t-t_3)\right], \tag{5}$$

$$V_{C_P}(t) = -\frac{V_S}{4}\left(1 + e^{-\zeta\omega_n(t-t_3)}\left(\cos(\omega_d(t-t_3)) + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left[\omega_d(t-t_3)\right]\right)\right).$$

Mode 5 (t_4<t<t_5) Gas-discharge Mode: Switch S_{M2} transfers the energy in C_1+C_2 to C_P via path S_{M2}-C_1-C_2-C_P. If the peak voltage reached in C_P in previous stage is:

$$V_{C_{P\_peak}} = -\frac{V_S}{4}\left(1 - \frac{e^{-\pi\zeta}}{\sqrt{1-\zeta^2}}\right). \tag{6}$$

Then, the difference between the peak voltage during t_3<t<t_4 and the voltage in t_4<t<t_5 is as follows:

$$\Delta V = -{V_S}/{2} - V_{C_{P_{peak}}} = -\frac{V_S}{4} - \frac{V_S \cdot e^{-\pi\zeta}}{4\sqrt{1-\zeta^2}}. \tag{7}$$

Mode 6 (t_5<t<t_6) Predischarge Mode: Switch S_{2b} is closed and therefore the energy stored in C_2 and L_{ERC} is transferred to C_P via path C_2-S_{2b}-D_{2a}-L_{ERC}-C_P in a resonant mode. Then, the current trough L_{ERC} and voltage panel C_P are:

$$I_{L_{ERC}}(t) = \frac{V_S}{4}\cdot\frac{1}{Z_r\sqrt{1-\zeta^2}}\cdot e^{-\zeta(t-t_5)}\cdot\sin\left[\omega_d(t-t_5)\right], \tag{8}$$

$$V_{C_P}(t) = -\frac{V_S}{4}\left(1 - e^{-\zeta\omega_n(t-t_5)}\left(\cos(\omega_d(t-t_5)) + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left[\omega_d(t-t_5)\right]\right)\right).$$

It is noted that in Mode 2 and Mode 5 the immediate change of the panel voltage is a significant source of oscillations in the panel waveforms and therefore, causing switching power losses. This change, in the case of Mode 2, is defined as follows:

$$\partial V_P = \frac{V_S}{4}\left(1 - \frac{e^{-\pi\zeta}}{\sqrt{1-\zeta^2}}\right). \tag{9}$$

3. COMPARATIVE ANALYSIS

The proposed architecture features less device voltage stresses compared with those of the conventional circuit [5] and similar to another multilevel sustaining driver [8].

3.1. Conduction Losses and Stress on Devices

For fair comparison, all the device voltages and currents ratings were based on the architecture diagram (showing in fig. 1), and using the conditions imposed in [4, 5, 8]. Table I shows the comparison of the component number and device stresses. The gas-discharge peak-current in the PDP is defined as I_{gas}. Is easily to note that, as in [8], the peak values as well as the rms values of each device current are appreciably reduced in the order of a half. However, it is imperative to note that the part count numbers used are six for the proposed circuit, eight for another multilevel topology and four for the conventional circuit. Thus, it is expected that the proposed architecture achieve a superior performance not just by the part count number, moreover due to the absence of a side-2 sustaining driver. As can be distinguish (Table II), the power losses are larger reduced due to the count part number.

3.2. Switching Losses

The immediate change of the panel voltage, (eq. 9), is a significant source of oscillations in the panel waveforms and therefore, causing switching power losses.

By performing similar analysis, we can obtain the turn-on losses in the sustaining switches as:

$$P_S \cong 2(C_{ds} + C_p)\cdot\partial V_p^2\cdot f\cdot \#\,devices \tag{10}$$
$$= \frac{(C_{ds} + C_p)\cdot\partial V_p^2\cdot f}{2}\left(1 - \frac{e^{-\pi\zeta}}{\sqrt{1-\zeta^2}}\right)^2\cdot \#\,devices.$$

In addition, the turn-on switching losses on the ERC switches are as follows:

$$P_{ERC} \cong \frac{C_{ds\text{-}ERC}\cdot V_{ds,pk\_ERC}^2}{2}\cdot f\cdot \#\,devices \tag{11}$$
$$= \frac{C_{ds\text{-}ERC}\cdot V_S^2\cdot f}{4}\cdot \#\,devices.$$

where C_{ds} and C_p are the inherent capacitances of the sustain switch and panel, respectively, and $C_{ds\text{-}ERC}$ is the drain to source capacitance of the ERC switches. Is expected that switching loss of the proposed circuit is smaller that the previous proposed circuits.

4. EXPERIMENTAL RESULTS

Figure 3(a-d) shows the correspondent experimental results using a pure capacitance; gate signals are FPGA-based. As seen in figure 3(c-d), it is noted that the turn-on switching losses can be negligible since the switches S_{1a}, S_{2a}, S_{M1} and S_{M2} operate nearly under the zero voltage switching condition.

4.1. *Practical Implementation*

In order to validate the features of the proposed topology, a prototype is implemented to drive a 42" PDP. As considered in [8, 9], the duration of T_{SUS} can be arbitrarily chosen in the range of 1.7–2.5$\mu sec.$ to be longer than the gas discharge extinction time. Figure 4 shows the experimental waveforms for a 42" PDP. It is easily appreciated in this bread boarded prototype the gas discharge current and the capacitive displacement waveform.

5. CONCLUSION

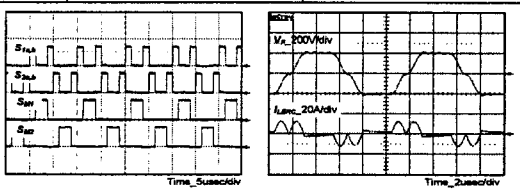
The comparative analysis gives a fine reason to consider this circuit as an alternative architecture related on multi-level sustaining drivers for plasma panels without much increased number of semiconductor devices. Therefore, it is reasonable to consider this circuit as a good candidate for a design of a low-cost high-power-density AC-PDP driver.

TABLE I
DEVICE NUMBER & STRESS COMPARISON

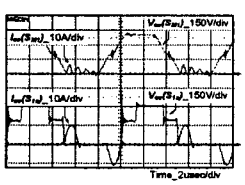
		Proposed Architecture	Multilevel Circuit[11]	Conventional circuit[4]
Total Number of Devices		6	16	8
Sustain switch	peak voltage V_{pk_sus}	$0.5V_S$	$0.5V_S$	V_S
	peak current I_{pk_sus}	I_{gas}	I_{gas}	I_{gas}
	RMS current I_{RMS_sus}	$V_S/4\sqrt{T_r f/2}$	$V_S/4\sqrt{T_r f/2}$	...
ERC switch	peak voltage $V_{pk\text{-}ERC}$	$0.25V_S$	$0.25V_S$	$0.5V_S$
	peak current $I_{pk\text{-}ERC}$	$V_S/4Z_r$	$V_S/4Z_r$	$V_S/2Z_r$
	RMS current $I_{RMS\text{-}ERC}$	$V_S/8Z_r\sqrt{T_r f}$	$V_S/8Z_r\sqrt{T_r f}$	$V_S/2Z_r\sqrt{T_r f}$
ERC Diode	peak voltage $V_{D,\,pk\text{-}ERC}$	$0.25V_S$	$0.25V_S$	$0.5V_S$
	peak current $I_{D,\,pk\text{-}ERC}$	$V_S/4Z_r$	$V_S/4Z_r$	$V_S/2Z_r$
	RMS current $I_{D,\,RMS\text{-}ERC}$	$V_S/8Z_r\sqrt{T_r f}$	$V_S/8Z_r\sqrt{T_r f}$	$V_S/2Z_r\sqrt{T_r f}$
	average current $I_{D,\,ave\text{-}ERC}$	$0.5CV_S f$	$0.5CV_S f$	$CV_S f$
Inductor	RMS current $I_{RMS\text{-}LERC}$	$V_S/4Z_r\sqrt{T_r f/2}$	$V_S/4Z_r\sqrt{T_r f/2}$	$V_S/Z_r\sqrt{T_r f}$
Capacitor	peak voltage $V_{pk\text{-}sus}$	$0.25V_S$	$0.25V_S$	$0.5V_S$
	RMS current $I_{RMS\text{-}sus}$	$V_S/4Z_r\sqrt{T_r f/2}$	$V_S/4Z_r\sqrt{T_r f/2}$	$V_S/Z_r\sqrt{T_r f}$
Clamp diode	peak voltage $V_{pk\text{-}sus}$	...	$0.5V_S$	...

TABLE II
CONDUCTION LOSS COMPARISON

Conduction Power Losses		**Proposed Architecture**	**Multilevel Circuit [11]**	**Conventional circuit**
Reactive Power	reactive power P_r	$0.5C_P V_S^2 f$	$0.5C_P V_S^2 f$	$C_P V_S^2 f$
ERC switches	$(I_{RMS\text{-}ERC})^2 \cdot R_{on\text{-}ERC} \cdot \#\ dev.$	$V_S^2/32Z_r^2 \cdot T_r \cdot f \cdot R_{on\_ERC}$	$V_S^2/16Z_r^2 \cdot T_r \cdot f \cdot R_{on\_ERC}$	$V_S^2/2Z_r^2 \cdot T_r \cdot f \cdot R_{on\_ERC}$
ERC Diode	$(I_{D,\,RM\text{-}ERC})^2 \cdot R_D \cdot \#\ dev.$	$V_S^2/32Z_r^2 \cdot T_r \cdot f \cdot R_D$	$V_S^2/16Z_r^2 \cdot T_r \cdot f \cdot R_D$	$V_S^2/2Z_r^2 \cdot T_r \cdot f \cdot R_D$
	$0.7 \cdot I_{D,\,ave\_ERC} \cdot \#\ dev.$	$0.7C_P V_S f$	$0.7C_P V_S f$	$0.7C_P V_S f$
Sustain switches	$(I_{RMS\text{-}sus})^2 + (I_{gas\text{-}RMS})^2 \cdot R_{on\text{-}sus} \cdot \#\ dev.$	$V_S^2/64Z_r^2 \cdot T_r \cdot f + 4I_{gas\_RMS} \cdot R_{on\_sus}$	$V_S^2/16Z_r^2 \cdot T_r \cdot f + 4I_{gas\_RMS} \cdot R_{on\_sus}$	$2I_{gas\_RMS}^2 \cdot R_{on\_sus}$



a) Control signals. b) Panel Voltage V_P, Current I_{LERC}.



c) ZVC turn-on of S_{1a} and S_{M1}. d) ZVC turn-on of S_{2a} and S_{M2}.

Fig. 3 Experimental waveforms.

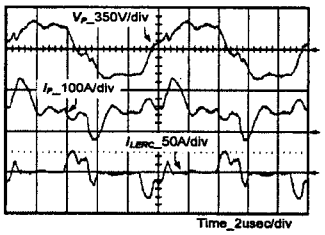


Fig. 4 Prototype of 42" PDP with MOSFET's.

REFERENCES

[1] S. K. Han, J. Y. Lee, G.W. Moon, M. J. Youn, C. B. Park, N. S. Jung, and J. P. Park, "Energy-recovery circuit for plasma display panel," *Electron. Lett.*, vol. 38, no. 15, pp. 790–792, Jul. 2002.

[2] S. K. Han, G. W. Moon, and M. J. Youn, "Current-fed energy-recovery circuit for plasma display panel," *Electron. Lett.*, vol. 39, pp. 1035–1036, Jul. 2003.
[3] L. F. Weber and M. B. Wood, "Energy recovery sustain circuit for the AC plasma display," in *Soc. Information Display Dig. (SID'87)*, vol. 7, 1987, pp. 92–95.
[4] L. F. Weber and M. B. Wood, "Energy recovery sustain circuit for the ac plasma display," in *Proc. Symp. Soc. Information Display*, 1987, pp. 92–95.
[5] H. Tottori, E. Hatabe, F. Isogai, and S. Yoshida, "A driving circuit for plasma display panels," in *Soc. Information Display Dig. (SID'75)*, vol. 6, Apr. 1975, pp. 118–119.
[6] J. S. Lai, F. Z. Peng, "Multilevel Converters A New Breed of Power Converters," in *IEEE Trans. on Ind. Appl.*, vol. 32, May 1996, pp. 509–517.
[7] T. A. Meynard, H. Foch, "Multilevel Converters and Derived Topologies for High Power Conversion," in *EPE Journal,* vol. 3, pp. 99-106.
[8] C. W. Roh, H. J. Kim, S. H. Lee, and M. J. Youn, "Multilevel voltage wave-shaping display driver for ac plasma display panel application," *IEEE J. Solid-State Circ.*, vol. 38, no. 6, pp. 935–947, Jun. 2003.
[9] C. Punset, S. Cany, and J.-P. Boeuf, "Addressing and sustaining in alternating current coplanar plasma display panels," *J. Appl. Phys.*, vol. 86, no. 1, pp. 124–133, July 1999.
[10] H. B. Hsu, C. L. Chen, S. Y. Lin, and K. M. Lee, "Regenerative power electronics driver for plasma display panel in sustain-mode operation," *IEEE Trans. Ind. Electron.*, vol. 47, no. 5, pp. 1118–1124, Oct. 2000.