전압 체배 정류단을 갖는 부스트 입력형 하프브리지 DC/DC 컨버터를 위한 새로운 전류 스트레스 저감 기법

박홍선, 김정은, 문건우
한국과학기술원
Email: gwmoon@ee.kaist.ac.kr

Novel Current Stress Reduction Technique for Boost Integrated Half-Bridge DC/DC Converter with Voltage Doubler Type Rectifier

Hong-Sun Park, Chong-Eun Kim, Gun-Woo Moon
Korea Advanced Institute of Science and Technology (KAIST)

Abstract

a current stress reduction technique for a boost integrated half-bridge (BIHB) DC/DC converter with voltage doubler type rectifier is proposed for digital car audio amplifier application. In the proposed circuit, two external capacitors are added parallel to the rectifier diodes in the secondary side of the transformer to shape the primary and the secondary current like rectangular waveforms in every switching instance. The experimental results of a 200W industrial sample show that the peak primary current decreases about by 10A. Thus, the proposed technique shows improved high efficiency.

1. INTRODUCTION

Recently, a low voltage high current DC/DC converter with high efficiency is strongly required for digital car audio amplifier application. To meet this requirement, a conventional asymmetrically controlled BIHB converter with an output inductor is proposed in [1-5]. This converter has many desirable features such as small input and output filters, low EMI due to soft switching. However, it has high voltage stresses of the rectifier diodes and also it has many magnetic components. To overcome these drawbacks, voltage doubler type rectifier, instead of an output inductor, is applied to the output stage of an asymmetrically controlled BIHB converter in [6-8]. It has many advantages over the conventional BIHB converter such as no DC magnetizing current, low voltage stress and low turn-off oscillation of rectifier diodes, and a reduced number of magnetic components. Even though with these advantages, voltage doubler type BIHB converter has a problem of high peak currents at both the primary and the secondary side due to no output inductor and small leakage inductance.

To solve this problem, the current stress reduction technique is proposed for the voltage doubler type BIHB converter, in which two external capacitors are connected parallel to the rectifier diodes. These current stress reduction capacitors make the currents abruptly increase at both the primary and the secondary side in every switching instance to charge one capacitor and discharge the other capacitor simultaneously. With this process, the peak current of the primary and the secondary side greatly decreases so that high efficiency can be obtained with reduced conduction loss compared to the voltage doubler type BIHB converter.

2. OPERATIONAL PRINCIPLES

Fig. 1 shows the voltage doubler type BIHB DC/DC converter with the proposed current stress reduction technique. As shown in Fig. 1, current stress reduction capacitors, C_1 and C_2, are added parallel to the rectifier diodes in the secondary side of the transformer and an asymmetrically controlled half-bridge converter integrated with a boost converter is employed in the primary side.

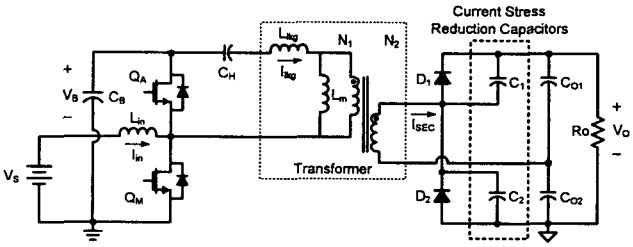

Fig. 1 Circuit diagram of the proposed converter

A. Mode analysis

The operational modes of the proposed converter are very similar to those of the BIHB converter with voltage doubler type rectifier in [6-8]. The distinct difference, as shown in Fig. 2 (c) and Fig. 3, is that currents build up abruptly at both the primary and secondary side in every switching instance in order to discharge one capacitor and charge the other capacitor simultaneously before the corresponding rectifier diode is turned on. The proposed converter operates in the eight modes that can be divided into two parts: t_0~t_4 and t_4~t_8 (=t_0). Operational principles of these two parts are so symmetric, thus the mode analysis for only the first part (t_0~t_4) will be given for simplicity.

Mode 1 (t_0~t_1): When the auxiliary switch, Q_A, is turned off at t_0, mode 1 begins as shown in Fig. 2 (a). During this mode, the drain-to-source current of Q_A, $I_{DS}(Q_A)$, decreases toward zero while the voltage of Q_A increases to V_B. The drain-to-source current of Q_M, $I_{DS}(Q_M)$, reversely flows through the parasitic body diode of Q_M while holding the drain-to-source voltage of Q_M zero.

Mode 2 (t_1~t_2): When the main switch, Q_M, is turned on at t_1, mode 2 begins as shown in Fig. 2 (b), where Q_M is turned on at ZVS condition. In this mode, the primary current, I_{lkg}, still flows to the negative direction as before and the current through D_2, $I_{D(D2)}$, decreases toward zero.

Mode 3 (t_2~t_3): Mode 3 begins when I_{lkg} changes its direction from the negative to the positive. As shown in Fig. 3, abrupt build-up of current occurs both at the primary and the secondary sides to discharge C_1 and to charge C_2. These two capacitors, called current stress reduction capacitors in this paper, make the primary and the secondary current waveforms change from the ramp type to the rectangular type. With this process, the peak values of the primary current and the secondary current can decrease. Fig. 4 shows the equivalent circuit for this mode, where the secondary current, $I_{SEC}(t)$, builds up rapidly until the voltage of the equivalently shown current stress reduction capacitor, C_1+C_2, is equal to output voltage with the following equation:

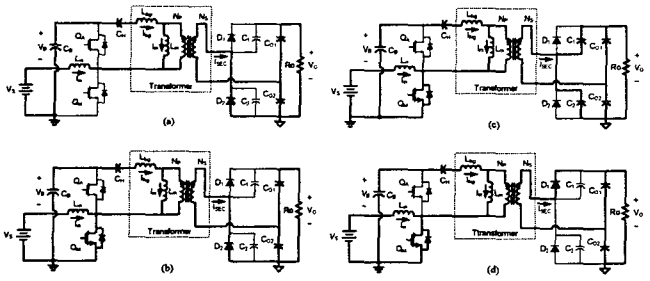

Fig. 2 Operational modes of the proposed converter, (a) Mode 1 (b) Mode 2 (c) Mode 3 (d) Mode 4

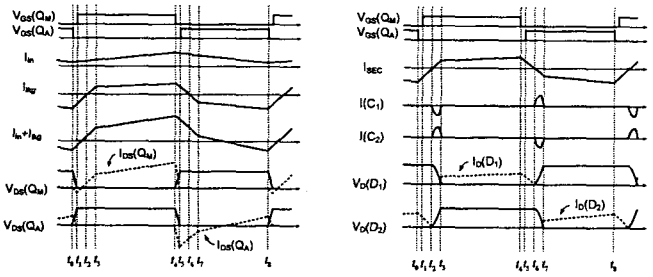

Fig. 3 Key waveforms of the proposed converter

$$I_{SEC}(t)=\frac{\eta V_S+DV_O}{\eta\sqrt{L_{lkg}/(C_1+C_2)}}\sin(\omega t), \tag{1}$$

where $t_2 \le t \le t_3 = t_2 + \frac{1}{\omega}\cos^{-1}\left(\frac{\eta V_S-(1-D)V_O}{\eta V_S+DV_O}\right)$, $\eta = N_2/N_1$, $\omega = \frac{1}{\eta\sqrt{L_{lkg}\cdot(C_1+C_2)}}$.

Mode 4 (t_3~t_4): Mode 4 begins when D_1 is turned on after C_1 and C_2 fully discharges and charges, respectively as shown in Fig. 3. During this mode, energy is transferred from the primary to the secondary side.

B. Input-output voltage conversion ratio

To obtain input-output voltage conversion ratio of the proposed converter, it is assumed that the voltages across C_B, C_H, C_{O1}, and C_{O2}, are constant during the switching period of T_S and the transient interval between turn-off of one switch and turn-on of the other switch is so narrow to ignore. By the inductor volt-second balance principle, the following equations can be obtained easily, where D is the duty ratio of Q_M.

$$V_B=\frac{1}{1-D}V_S \tag{2}$$

$$V_H=DV_B=\frac{D}{1-D}V_S \tag{3}$$

$$V_{O1}=(1-D)V_O \tag{4}$$

$$V_{O2}=DV_O, \tag{5}$$

where V_H, V_{O1}, and V_{O2} is the voltage across C_H, C_{O1}, and C_{O2}, respectively.

In this work, since it is difficult to derive exact input-output voltage conversion ratio, approximated voltage conversion ratio is derived using several assumptions. As waveforms shown in Fig. 5, the interval from t_0 and t_2, to the switching period, is so small to neglect and the rising time of the secondary current during the mode 3 is so short to treat the sinusoidal curve as a straight line even though its exact current wave can be obtained by equation (1).

To obtain approximated voltage conversion ratio, two peak values of the secondary current are necessary as indicated by p_1 and

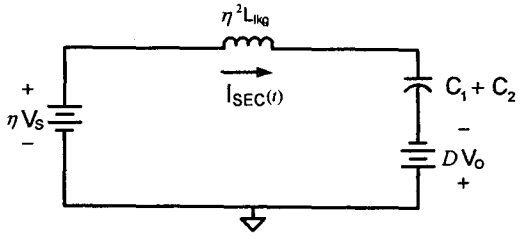

Fig. 4 Equivalent circuit of the mode 3

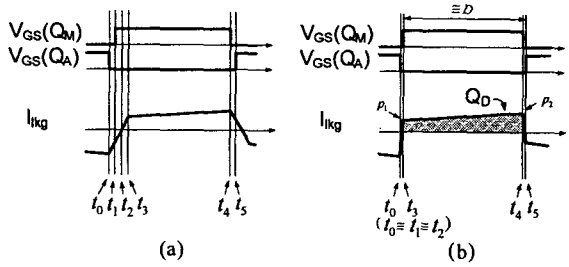

Fig. 5 Operational approximations to obtain simple input-output voltage conversion ratio, (a) before applying assumptions (b) after applying assumptions

p_2 in Fig. 5, where p_1 is the maximum value of the boosting secondary current at the end of the mode 3 and p_2 is the peak value of the secondary current at the end of the mode 4, respectively. The first value can be easily obtained using the equation (1) with the assumption of $t_3=\pi/2\omega$ as

$$p_1=I_{SEC}(t_3)=\frac{\eta V_S+DV_O}{\eta\sqrt{L_{lkg}/(C_1+C_2)}}\sin(\omega t)$$
$$=\frac{\eta V_S+DV_O}{\eta\sqrt{L_{lkg}/(C_1+C_2)}}. \tag{6}$$

And the second one can be obtained using the following equation with the assumption of t_4-$t_3=DT_S$ as

$$p_2=I_{SEC}(t_4)=\frac{\eta V_S-(1-D)V_O}{\eta^2 L_{lkg}}DT_S. \tag{7}$$

When applying voltage doubler type rectification to the output stage, it is satisfied that the total charge quantity through one of rectifier diodes during the turn-on interval should be equal to the product of load current and switching period.

$$Q_D=Q_{T_S}=I_O T_S=\frac{V_O}{R_O}T_S \tag{8}$$

$$Q_D=\frac{1}{2}\cdot DT_S\cdot\left\{2\frac{\eta V_S+DV_O}{\eta\sqrt{L_{lkg}/(C_1+C_2)}}+\frac{\eta V_S-(1-D)V_O}{\eta^2 L_{lkg}}DT_S\right\}, \tag{9}$$

where Q_D is the total charge quantity though D_1 shown in Fig. 5 (b). From the equation (8) and (9), the input-output voltage conversion ratio of the proposed converter can be obtained as

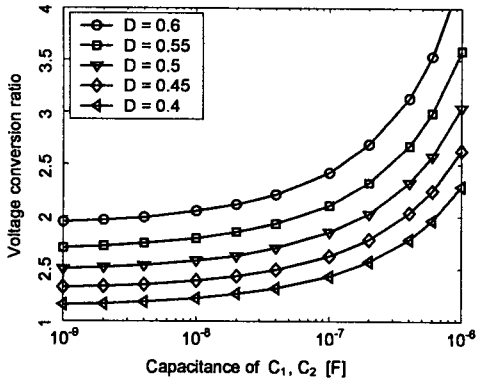

Fig. 6 Voltage conversion ratio vs. current stress reduction capacitor, C_1 and C_2, at T_S=12.5μs, L_{lkg}=0.9μH, R_O=3.125Ω, and η=1

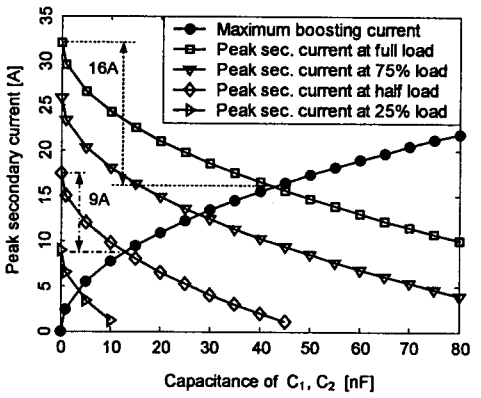

Fig. 7 Peak secondary current vs. current stress reduction capacitor, C_1 and C_2, under PWM control

$$\frac{V_O}{V_S} = 2\frac{\eta D\left(DT_S + 2\eta\sqrt{L_{lkg}\cdot(C_1+C_2)}\right)}{D^2\left((1-D)T_S - 2\eta\sqrt{L_{lkg}\cdot(C_1+C_2)}\right) + \dfrac{2\eta^2 L_{lkg}}{R_O}} \quad (10)$$

Above equation is plotted in Fig. 6, where it is remarkable that the higher capacitance of current stress reduction capacitors can provide the higher voltage conversion ratio.

C. *Current stress reduction of the proposed converter*

Compared to the voltage doubler type BIHB converter in [6-8], the proposed converter can greatly reduce the peak values of both the primary and the secondary currents. It comes from the fact that abrupt build-up of current occurs to discharge one capacitor and charge the other capacitor in every switching instance. Such current build-up makes the current waveforms change from the ramp type to the rectangular type at both sides. Fig. 5 shows one of exemplary secondary current waveforms of the proposed converter. In this figure, we can ensure that the peak value of rectangular type secondary current of the proposed converter be lower than that of ramp type secondary current of the conventional voltage doubler type BIHB converter without current stress reduction capacitor. And such reduction of peak current will go on until the maximum value of the boosting current after turn-on of a switch is equal to the peak value of current just before turn-off of the switch.

Fig. 7 shows that peak current of the proposed converter versus capacitance of the externally added capacitors. These results are extracted from the equation (8) and (9) and intuitively we can imagine from the equation (9) that the second term will decrease as much as the first term increases. In this figure, it is assumed that when not adding the current stress reduction capacitors, the maximum duty ratio of the main switch, Q_M, is an half at full load current of 8A with η=1.

As expected, the secondary current builds up rapidly with respect to increase of capacitance of the externally added capacitors. And with this phenomenon, the peak value of secondary current decreases gradually. Although the results in Fig. 7 comes from many assumptions, the peak secondary current in the voltage double type BIHB converter with the current stress reduction capacitors can maximally decrease by 16A and 9A at full load and half load, respectively if the capacitances of C_1 and C_2 are properly chosen.

3. EXPERIMENTAL RESULTS

To verify the operational principles and validity of the proposed technique, an industrial sample of the voltage doubler type BIHB converter employing the proposed current stress reduction technique is implemented.

The design specifications and circuit parameters of an industrial sample are summarized at TABLE I and TABLE II, respectively. For a careful comparison, an additional sample of the conventional voltage doubler type BIHB converter in [6-8] is also implemented.

TABLE I
DESIGN SPCIFICATIONS OF AN INDUESTIAL SAMPLE

Specifications	Value
Input voltage, V_S	10V ~ 16V, 14V normal
Output voltage, V_O	25V
Max. output power, $P_{O,max}$	200W
Switching frequency, f_S	80kHz

TABLE II
CIRCUIT PARAMETERS OF AN INDUESTIAL SAMPLE

Parameter	Value
Power switch, Q_M , Q_A	F3805, 2EA, 1EA
Rectifier diode, D_1, D_2	40CTQ045
Current stress reduction capacitor, C_1, C_2	47nF, MKP
C_B	1000μF, 35V, 3EA
C_S	47μF, 2EA
C_{O1} ,C_{O2}	1000μF, 35V, 2EA
L_{IN}	7.8μH
Transformer	N_1:N_2 = 4:4
	L_M = 20.6μH
	L_{lkg} = 0.45μH

In this sample, turns ratio of a transformer, N_1:N_2, is replaced with 3:4 to obtain the desired output voltage in the vicinity of half duty ratio just like the proposed circuit and input inductance, L_{IN}, increases to 23μH to reduce conduction loss in the primary side.
Fig. 8 shows the experimental waveforms of the industrial sample employing the proposed current stress reduction technique. As expected, main and auxiliary switches, Q_M and Q_A, are operated at ZVS condition and two rectifier diodes, D_2 and D_2, are operated at the zero current turn-on and turn-off with low voltage stresses and low voltage oscillations. It is noted that the current ringing through the two rectifier diodes is caused by current measuring extended wires.

Fig. 9 shows comparative primary current waveforms between the proposed converter and the conventional voltage doubler type BIHB converter. As shown in Fig. 9, the proposed voltage doubler

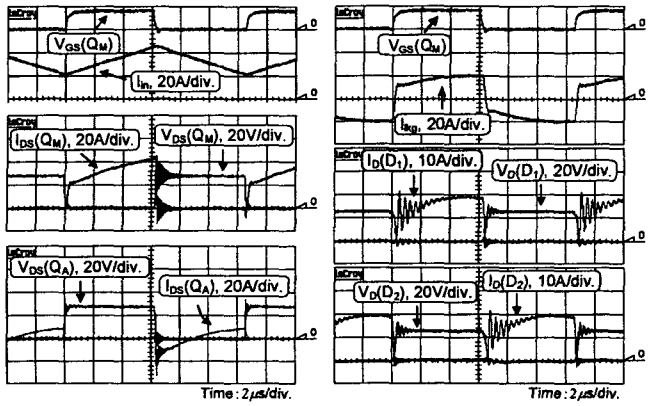

Fig. 8 Experimental waveforms of an industrial sample employing the proposed current stress reduction technique

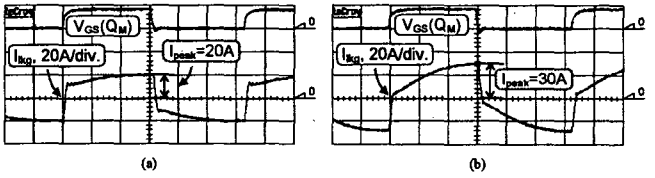

Fig. 9 Peak current comparison, (a) proposed converter (b) conventional voltage doubler type BIHB converter

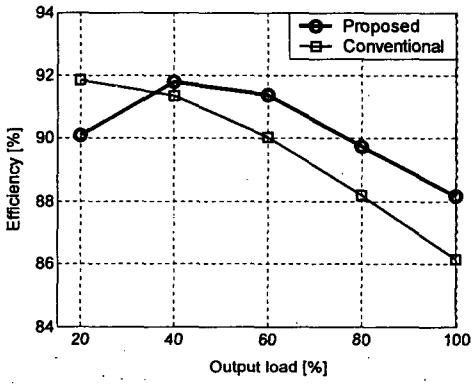

Fig. 10 Efficiency comparison at the nominal input voltage

type BIHB converter with the current stress reduction technique greatly reduces the peak primary current by 10A. Thus, 2% efficiency can be obtained for nearly entire load ranges expect for the light load condition as shown in Fig.10.

4. CONCLUSIONS

In this paper, the current stress reduction technique for a BIHB converter with voltage doubler type rectifier is proposed. This technique is just to add the external capacitors parallel to the rectifier diodes in the voltage doubler type output stage of the BIHB converter. With these externally added capacitors, abrupt build-up of current occurs to discharge one capacitor and charge the other capacitor simultaneously in every switching instance before the corresponding rectifier diode is turned on. With this process, the peak value of the secondary current remarkably decreases numerically and experimentally as shown in Fig. 7 and Fig. 9, respectively so that high efficiency can be obtained for nearly entire load conditions. The proposed converter can be widely applied to the low voltage and high current input systems such as digital car audio amplifier and battery sourced motor drive systems.

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