Ferroelectric properties of BLT films deposited on ZrO_2/Si substrates.

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Abstract : Metal-ferroelectric-insulator-semiconductor (MFIS) structures with $Bi_{3.35}La_{0.75}Ti_3O_{12}$ (BLT) ferroelectric film and zirconium oxide (ZrO_2) layer were fabricated on p-type Si(100). ZrO_2 and BLT films were prepared by sol-gel technique. Surface morphologies of ZrO_2 and BLT film were measured by atomic force microscope (AFM). The electrical characteristics of Au/ZrO_2/Si and Au/BLT/ZrO_2/Si film were investigated by C-V and I-V measurements. No hysteretic characteristics was observed in the C-V curve of the Au/ZrO_2/Si structure. The memory window width in C-V curve of the Au/BLT/ZrO_2/Si diode was about 1.3 V for a voltage sweep of ±5 V. The leakage current of Au/ZrO_2/Si and Au/BLT/ZrO_2/Si structures were about $3x10^{-8}$ A at 30 MV/cm and $3x10^{-8}$ A at 3 MV/cm, respectively.

Key Words : ZrO2, BLT, sol-gel, MFIS, Ferroelectric

1. Introduction

As modern electronic devices such as mobile phone and notebook computers come to be popular, the demand for nonvolatile memory devices has been increased. So ferroelectric thin films have been popular much attention for the application of nonvolatile ferroelectric memories (NVFeRAM) from the view points of high speed operation and low power consumption [1,2]. However, there are some problems such as interdiffusion of constituent elements, degradation of crystalline quality of the ferroelectric film, formation of an unnecessary transition layer and so on. In order to solve these problems, MFIS structures in which an insulator layer is inserted between the ferroelectric film and Si substrate, have been generally used [3,4]. The insulator layer is used to prevent the reaction and interdiffusion between the ferroelectric layer and the silicon substrate as well as to improve the retention properties [5].

In this study, ZrO_2 films were formed on p-type Si(100) and BLT films were deposited on ZrO_2/Si structure by using sol-gel methode. ZrO_2 is used as a buffer layer between ferroelectric and Si, which has been studied for application to diffusion barriers and electrical insulators on microelectronics due to their high chemical stability and high resistivity [6]. In addition, It has been known that ferrelectric BLT also has advantages more than other ferroelectric thin films such as PZT [7], SBT [8] for using FeFET devices.

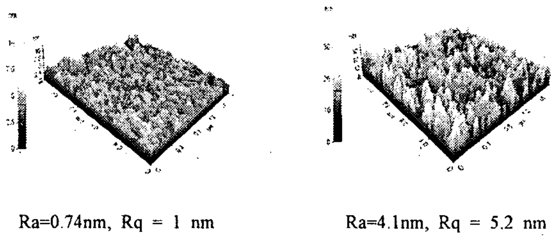
2. Experiments

To fabricate the MFIS diode, p-type Si(100) was used as a substrate. The substrate was dipped in HF solution to remove surface native oxide. As a buffer layer, ZrO_2 films were deposited on a substrate by sol-gel. It was spin- coated at 500 rpm for 5 s and 5000 rpm for 25 s. The coated films were dried at 240 ℃ for 10 minutes on hot plate to remove organic material. Then dried films were fired at 400 ℃ for 10 minutes in O_2 atmosphere by RTA and the films were crystallized at 700 ℃ for 10 minutes in O_2 atmosphere using RTA.

Next, BLT films also were deposited on ZrO_2/Si by sol-gel. The stoichiometry of the solution was $Bi_{3.35}La_{0.75}Ti_3O_{12}$. It was spin coated at 500 rpm for 5s and 3000 rpm for 25s. The coated films were dried at 240℃ for 10 minutes on hot plate to remove organic material. These processes. After several repetitions of these process to obtain designed film thickness, the films were annealed at 750℃ for 30 minutes in O_2 atmosphere by RTA. Then as an electrode, Au was deposited by thermal evaporator. The surface roughness of both ZrO_2/Si and BLT/ZrO_2/Si structures were analyzed by atomic force microscopy (AFM). Capacitance-voltage (C-V) and leakage current-voltage (I-V) characteristics were measured by 4280A and HP 4145B, respectively.

3. Results and Discussions

Fig. 1 shows the AFM image of ZrO_2/Si and BLT/ZrO_2/Si structure. The measure area was 2x2 um for both structures. The surface roughness of ZrO_2/Si were measured average (Ra) 0.74 nm and root-mean-square (RMS) 1 nm. The fabricated ZrO_2 film has very flat and smooth surface morphologies. Surface roughness of a buffer layer is very important because the surface structure of a buffer insulator affects the electrical properties of the MFIS structure. The surface roughness of BLT/ZrO_2/Si were measured average (Ra) 4.1 nm and root-mean-square (RMS) 5.24 nm, respectively. The measured values are indicated that it is a very good surface morphology.



Ra=0.74nm, Rq = 1 nm　　　　Ra=4.1nm, Rq = 5.2 nm

Fig. 1 AFM image of (a) ZrO_2 and (b) BLT films.

Next, the dielectric properties of ZrO_2 and BLT films were investigated by high frequency (1 MHz) C-V measurement. Fig. 2 shows a typical capacitance-voltage characteristic for Au/ZrO_2/Si(100) and Au/BLT/ZrO_2/Si structures. It is worth noting that no hysteretic loop was observed in Fig. 2(a). The equivalent oxide thickness (EOT) value derived from the accumulation capacitance was 7.5 nm. Fig 2(b) shows the hysteresis loops with a clockwise direction, as indicated by arrows. The value of the memory window width was about 1.3 V for the bias voltage with ±5 V sweep range. As can be seen in the Fig.2(b), along with the increase of bais voltage, values of memory window are increased.

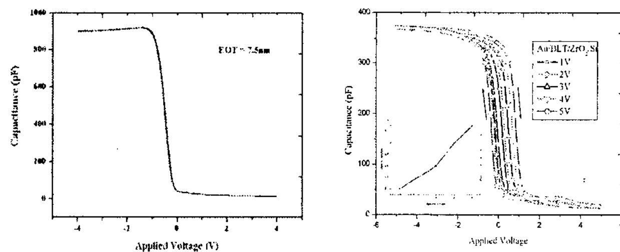


Fig. 2 Capacitance-volatage characteristics of Au/ZrO_2/Si MIS structure (a) and Au/BLT/ZrO_2/Si MFIS structure (b).

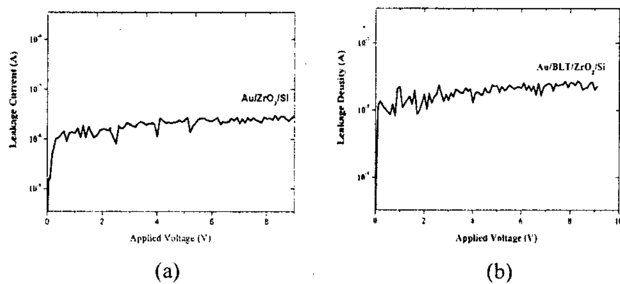


Fig. 3 Leakage current-voltage characteristics of Au/ZrO_2/Si MIS structure (a) and Au/BLT/ZrO_2/Si MFIS structure (b).

The value of current leakage density is about 3×10^{-8} A at 30 MV/cm. This result shows that the insulating property of the ZrO_2 film is excellent. Fig. 3(b) shows the value of current leakage density at 3 MV/cm is about 3×10^{-8} A, which indicates that the film provides good insulation.

4. Conclusion

We fabricated and measured MIS, MFIS capacitors. No hysteretic characteristic was observed in the C-V curve of the MIS structure. The hysteresis loop due to the BLT film's ferroelectricity was observed in the C-V characteristic of the MFIS structure. The memory window width of the BLT film was about 1.3 V for the sweep range of ±5 V. Along with increasing voltage, the values of memory widow increase. The current leakage density was about 3×10^{-8} A at 30 MV/cm of Au/ZrO_2/Si structure. The leakage current density value of Au/BLT/ZrO_2/Si structure was about 3×10^{-8} A at 3 MV/cm.

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