비소 고상확산방법을 이용한 MOSFET SOI FinFET 소자 제작

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Fabrication of SOI FinFET devices using Arsenic solid-phase-diffusion

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Abstract : A simple doping method to fabricate a very thin channel body of the *n*-type fin field-effect-transistor (FinFET) with a 20 nm gate length by solid-phase-diffusion (SPD) process is presented. Using As-doped spin-on-glass as a diffusion source of arsenic and the rapid thermal annealing, the *n*-type source-drain extensions with a three-dimensional structure of the FinFET devices were doped. The junction properties of arsenic doped regions were investigated by using the n^+-p junction diodes which showed excellent electrical characteristics. Single channel and multi-channel *n*-type FinFET devices with a gate length of 20-100 nm was fabricated by As-SPD and revealed superior device scalability.
Key Words : solid phase diffusion; ultra-shallow junction; nano-scale, FinFET; As-doped SOG

1. Introduction

As the dimension of silicon MOSFETs shrinks to sub-100 nm regime, reducing the short channel effects becomes major efforts for the further scaling down of nano-scaled complementary metal-oxide-semiconductor (CMOS) devices. To overcome the short channel effects, the FinFET is recently reported self-aligned double-gate structure [1]. However, three-dimensional device architecture of FinFET leads to more complicate processing especially the doping of source/drain extension regions in comparison with the conventional planar CMOS transistors [2]. The solid phase diffusion (SPD) process is an alternative doping method for three-dimensional device architecture and is known as a defect-free process [3]. In this study, we investigated the fabrication of *n*-type FinFET devices by arsenic SPD using a As-doped SOG(spin-on-glass) as diffusion source.

2. Experiments

The *p*-type SOI wafers with 200 nm buried oxide layer and 100 nm top silicon layer were used for *n*-type FinFET's fabrication. Silicon fin channels with a width of 20 nm were obtained by EBL and Cl_2-based inductively coupled plasma reactive ion etch (ICP RIE) process. A gate oxide with a thickness of 4 nm was grown by dry oxidation and an in-situ phosphorus-doped polysilicon film with a 100 nm thickness was deposited as a gate electrode using the low-pressure chemical-vapor deposition (LPCVD). Poly-Si gate electrode was formed by EBL and ICP RIE process. The silicon nitride film with 20 nm thickness was deposited by LPCVD and was etched back to form the sidewall spacer. A liquid-state dopant source containing arsenic was used as a SPD source. A liquid-type dopant source was changed to a solid-state As_2O_5 layer by baking processes in N_2 ambient. A rapid thermal annealing (RTA) with high ramp-up rate (+50°C/s) and ramp-down rate (-50°C/s) was carried out in N_2 ambient at 950°C for diffusing the arsenic to the source-drain extensions of *n*-type FinFET devices.

3. Results and Discussion

Figure 1 shows the SIMS profiles of arsenic for various temperatures of RTA process. The diffusion length of arsenic increased with increasing RTA temperature. However, the diffusion length of As is much shallower than that of P comparing our previous report [3].

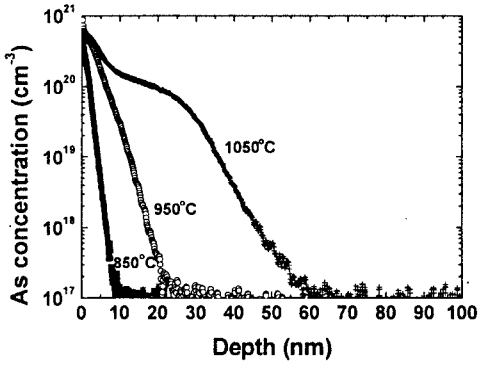

Figure 1. SIMS profiles of arsenic for various RTA process temperatures using by using arsenic SPD.

Figure 3 shows the current-voltage (I-V) characteristics of n^+-p diodes fabricated on the silicon substrate by SPD as a parameter of RTA temperature. The reverse bias current decreased with increasing temperature, because the junction

depth increase with diffusion temperature, which resulted in improvement of junction curvature. On the other hand, the forward bias current increased with RTA temperature, which is attributed to the reduction of resistance at arsenic doped region.

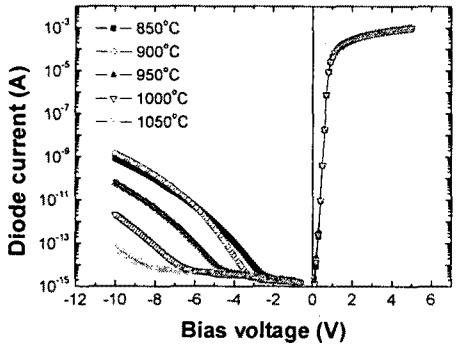

Figure 2. I-V characteristics of n^+-p diode fabricated on silicon substrate by arsenic SPD methods with the parameter of RTA temperature.

Figure 3 shows structure of fabricated single-channel FinFET devices with a 20 nm silicon fin width and gate length. The nitride sidewall spacer of gate electrode was 20 nm.

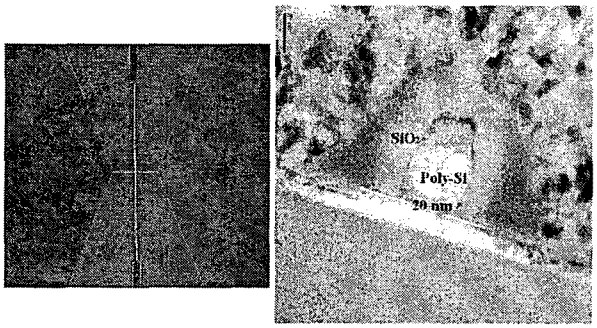

Figure 3. Plane-view SEM image (left) of fabricated FinFET with a 20 nm silicon fin width and cross-sectional TEM image of gate line (right).

Figure 4 shows the subthreshold current characteristics (I_d-V_g) for the *n*-type FinFET devices with 20 nm gate length. The arsenic SPD process was carried out by using the RTA at 950°C. The results of FinFET device showed excellent subthreshold characteristics even in 20 nm gate length. The subthreshold swing and DIBL (drain induced barrier lowering) for 100 nm gate length were 61.5 mV/dec and 10 mV, respectively. This subthreshold swing is almost same with ideal value of silicon MOSFET device (60 mV/dec). In case of 20 nm gate length, he subthreshold swing and DIBL (drain induced barrier lowering) for were 97.5 mV/dec and 220 mV, respectively.

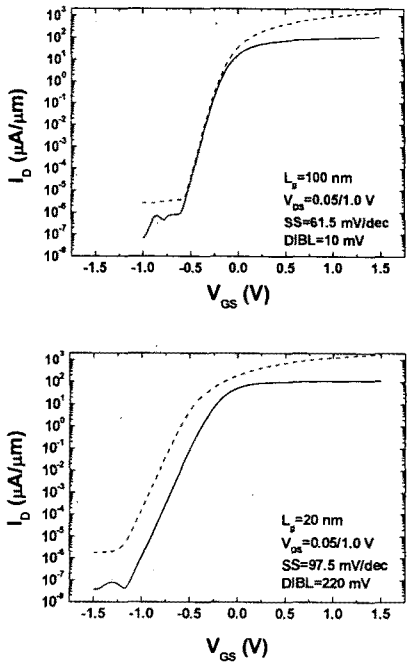

Figure 4. I_d-V_g characteristics of n-type FinFETs with 100 nm and 20 nm gate length.

4. Conclusions

A shallow-junction formation technique for the fabrication of n-type FinFET device with sub-100 nm gate length was reported. Using the arsenic SPD process with As-doped SOG diffusion source, the *n*-type FinFETs with gate length of 20-100 nm and the n^+-*p* junction diodes with extremely shallow junction depth were fabricated. Arsenic SPD was proved to be very effective process for sub-100 nm CMOS technology, because the n^+-*p* junction diodes with shallow junction depth and the n-type FinFET devices with a 20 nm gate length showed good electrical characteristics. Therefore, we concluded that the arsenic SPD process using the As-doped SOG is a promising doping technique for the further device scaling of nano-scale *n*-type FinFET devices.

References

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