

Fabrication and Characterization of the BLT/STA/Si Structure for Fe-FETs Application

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Abstract: Ferroelectric thin films have been widely investigated for future nonvolatile memory application. We fabricated the BLT ((Bi,La)₄Ti₃O₁₂) films on Si using a STA (SrTa₂O₆) buffer layer. BLT and STA film were prepared by sol-gel method. Measurement data by XRD and AFM, showed that BLT film and STA films were well crystallized and a good surface morphology. From C-V measurement reward that the Au/BLT/STA/Si structure showed a clockwise hysteresis loop with a memory window of 1.5 V for the bias voltage sweep of ± 5 V. From results, the Au/BLT/STA/Si structure is useful for FeFETs.

1. Introduction

Ferroelectric memories are promising as one of the future nonvolatile memories. In particular, one-transistor type Fe-FETs (ferroelectric-gate field-effect-transistors) have received much attention in terms of nondestructive read out and high-density implementation [1]. To fabricate Fe-FETs, ferroelectric materials have to be deposited of silicon substrates. However, the MFS (metal-ferroelectric-semiconductor) structure as a gate stack in Fe-FETs with has disadvantages such that the interfacial layer between ferroelectric thin film and silicon substrate is difficult to be controlled [2-3]. As one of the ways to overcome this problem, a buffer insulator such as LaAlO₃, ZrO₂ and HfO₂ is inserted at the interface between ferroelectric thin film and silicon substrate to fabricate the MFIS (metal-ferroelectric-insulator-semiconductor) structure [4-6].

In this work, we fabricated the Au/BLT/STA/Si structure as a MFIS structure in Fe-FETs. The STA (SrTa₂O₆) thin film was chosen as a buffer layer. The STA film has been recently investigated for application to electrical insulators in microelectronics owing to their high dielectric constant and good electrical properties [7,8]. In addition, BLT ((Bi,La)₄Ti₃O₁₂) films were deposited on STA/Si structures as a ferroelectric layer. Because of their fatigue-free characteristics and long retention properties, it has been suggested that BLT films among several ferroelectric materials, are suitable for Fe-FETs [9]. We evaluated the physical and electrical properties of the Au/BLT/STA/Si structure.

2. Experiments

STA thin film was prepared on p-type (100) silicon substrates by sol-gel. Prior to the STA, the native oxide layer on the surface of the Si wafers was removed by soaking into BOE (buffered oxide etchant). The STA was spin-coated at 5000rpm for 25 sec. The STA was baked at 380 °C for 10 min, and at 900 °C for 3 min in O₂ atmosphere by RTA (rapid thermal annealing). On STA/Si structure, BLT films were spin-coated at 3000 rpm for 20 sec using sol-gel techniques and dried at 250 °C for 10 min on a hot-plate. After repeating these processes to obtain the desired

thickness, the film was finally crystallized by annealing at 750 °C for 30 min in O₂ atmosphere. To investigate the electrical properties, Au electrodes were thermally evaporated onto the top and bottom sides of the samples.

The crystallinity of the Au/STA/Si MIS and the Au/BLT/STA/Si MFIS structure was characterized by XRD (x-ray diffraction) analysis. The C-V (capacitance-voltage) and J-V (current density-voltage) characteristics were measured with HP 4280A and HP 4145B, respectively.

3. Results and Discussion

The crystalline characteristics of the STA/Si structure and BLT/STA/Si structures were investigated. Figure 1 shows the XRD patterns of the STA/Si structure crystallized at 900 °C for 3 min in O₂ atmosphere (a) and (b) the BLT/STA/Si structure crystallized at 750 °C for 30 min in O₂ atmosphere. In figure 1(b), the STA thin film was fully crystallized that the BLT film on STA/Si structure well crystallized with STA strong (117) peak.

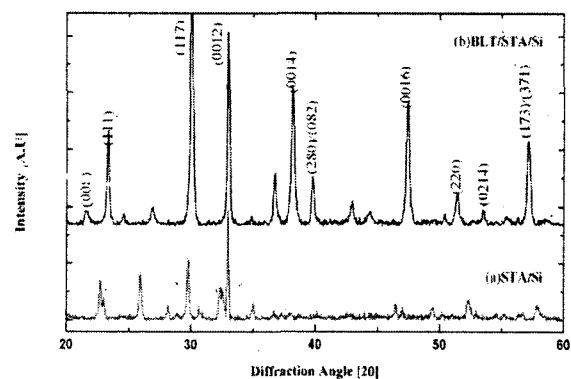


Figure 1. X-ray diffraction patterns of (a) the STA/Si structure, (b) the BLT/STA/Si structure.

Figure 2 Shows the surface AFM images. RMS(root mean square) roughness value of a STA thin film. It is well known that the surface roughness of buffer insulator is very important for ferroelectric properties of ferroelectric layer in MFIS structure. Thus, The very smooth surface of STA thin film was very encouraging result. For the BLT/STA/Si structure shown in (b), the RMS value was 9.02 nm. BLT film also has a good surface.

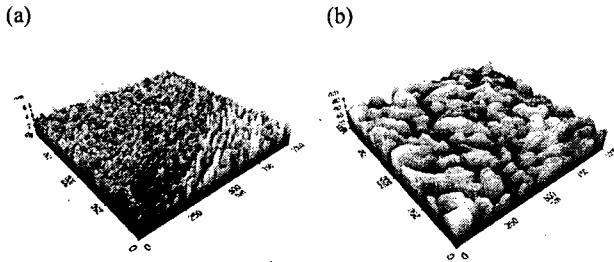


Figure 2. AFM images of (a) the STA film, (b) the BLT film.

Figure 3 shows the result of the high frequency (1 MHz) C-V measurement of STA/Si structure in 900 °C for 3 min in O₂ atmosphere. It should be noted that hysteric shift in curves for positive and negative bias sweeps was not observed, indicating little rechargeable oxide trap existed at the interface between STA and Si. The STA film has EOT of 5.7 nm and its calculated dielectric constant was about 16.5.

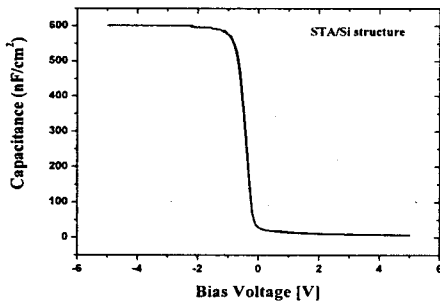


Figure 3. C-V characteristics of Au/STA/Si(MIS) structure.

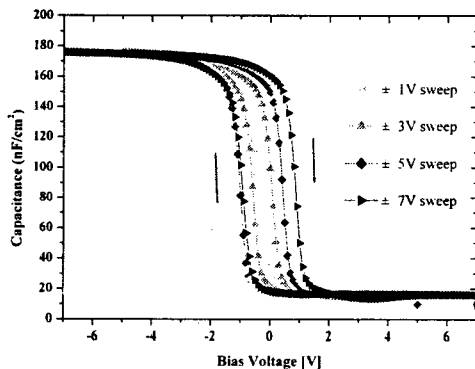


Figure 4. C-V characteristics of BLT/STA/Si(MFIS) structure.

Figure 4 shows the C-V characteristics for the BLT/STA/Si structure with the bias voltage. The memory window width increased with the increase of the applied bias voltage and 1.5 V BLT/STA/Si structure observed about 1.5 V for the bias sweep rang of ± 5 V.

Figure 5 shows the J-V characteristics of the Au/BLT/STA/Si MFIS structure and the Au/BLT/Si MFS structure. Leakage

current densities the Au/BLT/STA/Si MFIS structure and the Au/BLT/Si MFS structure were about 1×10^{-7} A/cm² and 5×10^{-7} A/cm² at 5 V, respectively. From these results, we knew that J-V characteristics were improved by using the STA film as a buffer layer.

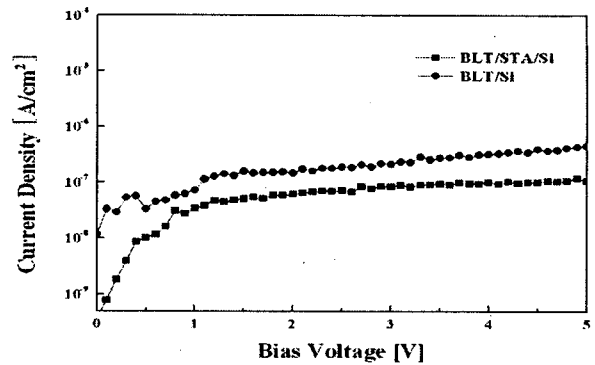


Figure 5. J-V characteristics of the Au/STA/Si structure, and the Au/BLT/Si structure.

4. Conclusions

In this study, we fabricated MFIS for electrical properties. STA films as a buffer layer no observed hysteresis property and EOT estimated to be about 5.7 nm. In Au/BLT/STA/Si MFIS structure, showed a memory windows width of about 1.5V the bias sweep rang of ± 5 V. Memory window of the MFIS structure increased with the increase of the applied bias voltage. The J-V property of the MFIS structures was improved by inserting the STA film.

References

- [1] J. F. Scott, *Ferroelectric Memories*, (Springer-Verlag, Germany, 2001).
- [2] B.-E. Park, and H. Ishiwara *J. Kor Phys. Soc.* 42, 1149 (2003).
- [3] B.-E. Park, K. Takahashi and H. Ishiwara, *J. Kor Phys. Soc.* 46, 346 (2005).
- [4] B.-E. Park, and H. Ishiwara, *Appl. phys Lett.* 79, 806 (2001).
- [5] J.-D. Park, J.-H. Choi and T.-S. Oh, *Jan. J Appl. phys.* 41, 5645 (2002)
- [6] B.-E. Park, K. Takahashi and H. Ishiwara, *Appl. phys Lett.* 85, 4448 (2004).
- [7] K. H. Park, H. S. Jeon, Z. W. Kim, B.-E. Park and C. J. Kim. *Pro. of the KIEEME Annual summer conference 2006.* Vol. 7, p. 198-199 (2006).
- [8] S. Regnery, R. Thomas, P. Ehrhart and R. Waser, *J. Appl. Phys.* Vol. 97, p. 073521, 2005.
- [9] B.-E. Park, B. S. Kang, S. D. Bu, T. W. Noh, J. Lee and W. Jo, *Nature* 401, 682 (1999)