Si-strained layer를 가지는 Silicon-Germanium on Insulator MOSFET에서의 이동도 개선 효과

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Improvement of carrier mobility on Silicon-Germanium on Insulator MOSFET devices with a Si-strained layer

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Abstract : The effects of heat treatment on the electrical properties of SGOI were examined. We proposed the optimized heat treatments for improving the interfacial electrical properties in SGOI-MOSFET. By applying the additional pre-RTA(rapid thermal annealing) before gate oxidation and post-RTA after dopant activation, the driving current, the transconductance, and the leakage current were improved significantly.

Key Words : SGOI MOSFET, Strained silicon channel, RTA, interface states, mobility enhancement

1. Introduction

As the gate lengths of MOSFETs scaled down to sub-100 nm regime, the operation is limited by the short-channel effects (SCE). The SOI devices relax the SCE compared to the bulk-silicon [1]. Especially, strained-Si/SiGe-on-insulator (SGOI) MOSFET attracts higher attention than the SOI MOSFET because of superior transport performance [2]. However, a limiting factor of SGOI substrates is the high density defects with increase of Ge content. Because SGOI devices have two interfaces at the gate oxide/strained-Si channel and the silicon channel/buried oxide, the device performance will be significantly affected by both interfacial electrical properties. In this work, we evaluated the interfacial electrical properties, particularly at the channel/buried oxide of SGOI substrate for the first time. Since the RTA process is one of the key technologies for an ultra-shallow junction formation in nano-scale CMOS device, effects of RTA and furnace annealing on the interfacial property and device performance of SGOI MOSFET as a function of Ge content was also investigated.

2. Experiments

Nano-scale thick strained-Si SGOI wafers were fabricated by low temperature epitaxial graded and buffered SiGe growth. CMP, hydrogen implantation, bonding, cleavage, and surface treatment processes were employed to fabricate nano-sclae SGOI substrate with a strained silicon channel. Finally, the strained silicon of 10nm was formed on the relaxed $Si_{1-x}Ge_x$ of 50 nm. The contents of Ge in relaxed $Si_{1-x}Ge_x$ layer were 0, 10, 15 and 20 %. N-channel SGOI MOSFET devices were fabricated to characterize the current transport characteristic depending on Ge content in SiGe layer. Dopant activation annealing of source/drain region was carried out at 850°C/30s in N_2 ambient by RTA. To improve the device performance of SGOI MOSFET, the pre-RTP at 900°C/30s was implemented before gate oxidation and the post-RTA at 500°C/30m in nitrogen ambient was followed after dopant activation annealing.

3. Results and Discussion

Figure 1 is the SEM images of SGOI n-MOSFET devices. To confirm the effectiveness of RTA and furnace annealing, RTA was carried out before gate oxidation and furnace annealing was carried out after dopant activation.

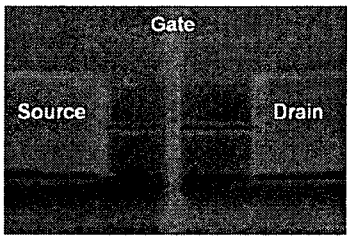

Figure 1. SEM images of SGOI n-MOSFET device.

Figure 2 is the I_d-V_g curves of SGOI n-MOSFET with 10 and 20 % Ge content. The results show the effects of applying RTA only, the pre-RTA process, and both the pre- and post-RTA processes. The the combination of the pre-RTA and post-RTA processes after source/drain activation annealing significantly enhanced the drain current by two orders of magnitude as compared to that with FA process only.

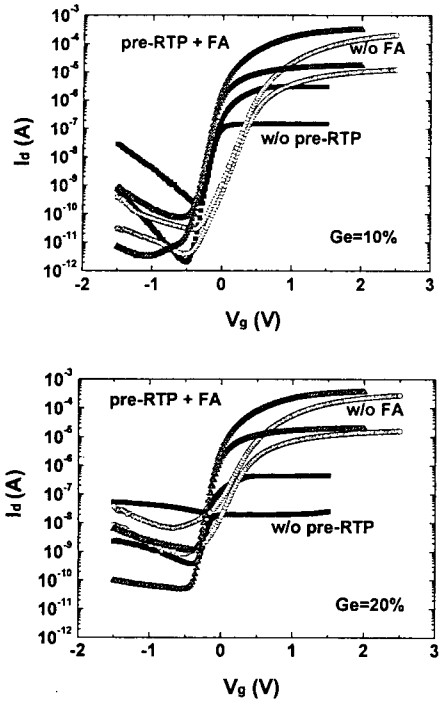

Figure 2. I_d-V_g characteristics obtained from the SGOI n-MOSFET devices for 10 % Ge content, and 20 % Ge content. Closed squares correspond to without the pre-RTA treatment before gate oxidation, and open circles correspond to the pre-RTA treatment. Closed triangles correspond to the combination of pre-RTA before gate oxidation and post-RTA furnace annealing (FA) after source/drain activation.

Figure 3 is the I_d-V_{ds} curves of SGOI n-MOSFET with 0, 10, 15 and 20 % Ge content after the pre-RTA and post-RTA processes. The drain current increased with the Ge due to the mobility enhancement of electrons in the strained-Si inversion layer [3].

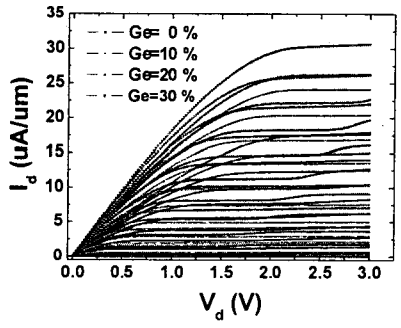

Figure 3. I_d-V_{ds} characteristics obtained from the SGOI n-MOSFET devices for 0 %, 10 %, 15 % and (b) 20 % Ge content in relaxed $Si_{1-x}Ge_x$ layer.

Figure 4 shows the field effect mobility of SGOI n-MOSFET devices as a function of Ge. The enhancement mobility was 3 %, 19 % and 48 % for 10 %, 15 % and 20 % Ge contents, respectively, as shown in Table. 1.

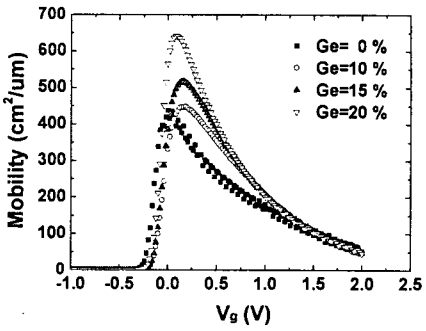

Figure 4. Enhancement of electron mobility in strained-Si MOSFET as a function of Ge content of relaxed SiGe layer in SGOI substrates.

Table 1. Enhancement of field effect mobility of SGOI n-MOSFET as a function of Ge contents .

Ge content (%)	Mobility (cm^2/Vs)	Enhancement (%)
0	435	-
10	447	2.8
15	517	18.9
20	641	47.4

4. Conclusions

In summary, we found that as the Ge concentration increased the electric characteristics of strained-Si channel SGOI n-MOSFETs were degraded. By applying the additional pre-RTA process, the driving current, the transconductance, and the leakage current were significantly improved. The additional post-RTA process, consisting of 30 min in a N_2 ambient at 500°C, was very effective in improving the electrical characteristics of nano-scale strained-Si channel SGOI n-MOSFETs.

References

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