Low Power and Small Area Holding Latch with Level Shifting Function Using LTPS TFTs for Mobile Applications

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Abstract

A holding latch with level shifting function is proposed for power and cost effectiveness with low temperature polycrystalline silicon technology on the glass backplane. Layout area and power consumption of the proposed circuit are reduced by 10% and 52% compared with those of the typical structure which combines a static D-latch and a cross coupled level shifter for 2.2" qVGA panel, respectively.

1. Introduction

Recently, the market of mobile devices such as cellular phones, personal digital assistants(PDAs), and portable multimedia players(PMPs) has rapidly grown up. Moreover, customers want mobile devices with high performance display specifications which are compact size, low power consumption, high resolution, and high quality images. To realize compact size display, system-on-a-panel(SoP) using low temperature poly-Si (LTPS) thin film transistors(TFTs) is considered as promising solution because the LTPS TFT has higher carrier mobility than the a-Si TFT, which allows driving circuitries to be integrated directly on the glass backplane[1][2].

Layout area and power consumption are most important issues in the mobile display technology because of its compactness and the battery capacity in mobile applications. Especially, a level shifter that changes low voltage swing signals to high voltage swing signals for a digital-to-analog converter (DAC) in an integrated data driver on a panel consumes large amount of power because every channel needs N level shifters in the N-bit gray scale display system. Thus the level shifter block occupies large area as well as it consumes high power.

Figure 1 shows the holding latch of the static D-latch structure and the cross coupled level shifter for a typical data driver. To reduce layout area, the combined structure of two circuit, a holding latch and a level shifter, has been proposed[4], but power consumption is still a problem because it uses a high voltage inverter chain instead of a level shifter which controls the power supply while low voltage data is converted to high voltage. Therefore, a control block, outside of source driver, needs large driving capability and consumes large power.

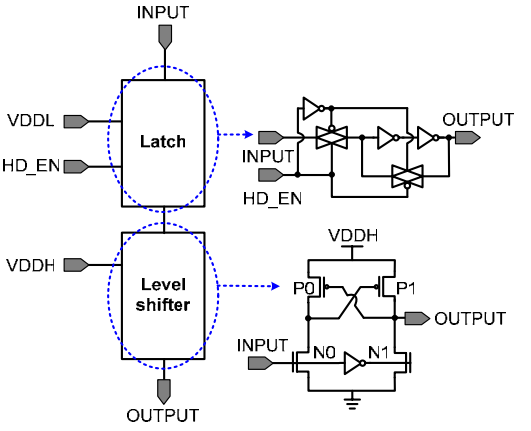


Figure 1. Conventional holding latch and level shifter.

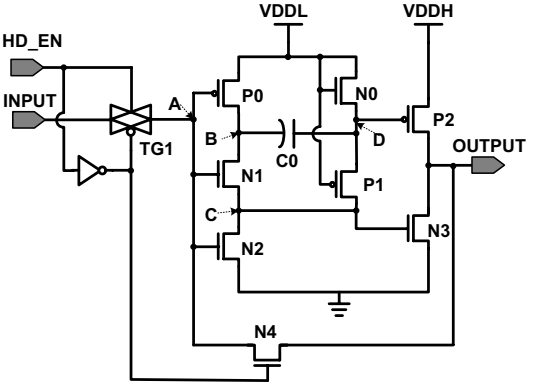


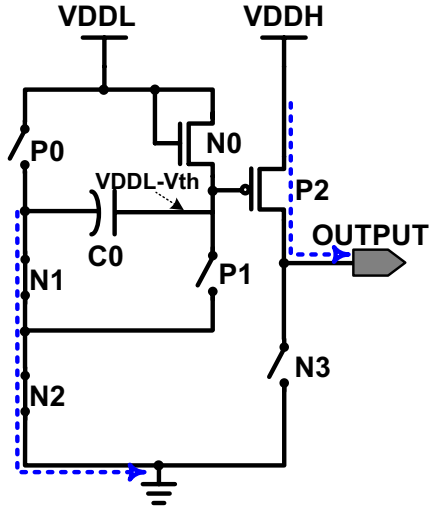
Figure 2. Schematic diagram of proposed circuit.

We propose an area-efficient and low-power holding latch with level shifting function.

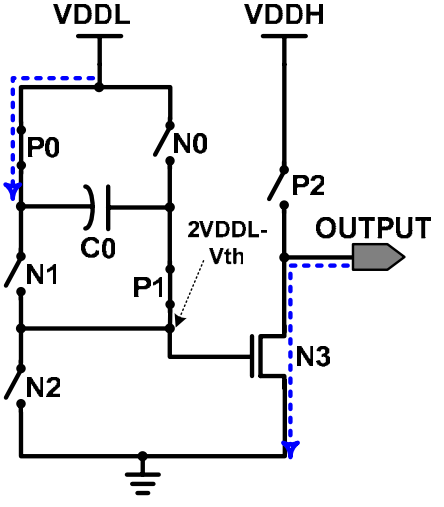
2. Proposed Circuit

The schematic diagram of the proposed circuit is shown in Figure 2. The structure of this circuit uses an inverter chain to store data like a conventional D-latch, and prevents high voltage data from flowing backward by capacitance coupling effect.

The VDDL is low supply voltage, and VDDH is high supply voltage. When INPUT becomes VDDL from GND while HD_EN signal is HIGH, node A becomes VDDL, and then node B and C drop to GND since P0 is turned off, N1 and N2 are turned on.



(a)



(b)

Figure 3. Operation of the proposed circuit (a) storing HIGH state, (b) storing LOW state.

Because N0 is diode-connected, node D becomes VDDL-Vth, where Vth is the threshold voltage of N0. Thus, the output of the circuit charges to VDDH as P2 is turned on. Figure 3 (a) describes a HIGH state storing operation.

After that, when HD_EN signal changes its state to LOW, HIGH state is stored because N4 prevents node A from being GND. If node A becomes less than VDDL-Vth1, where Vth1 is the threshold voltage of N4, node A and OUTPUT are shorted by N4, so node A keeps HIGH state.

In the opposite case, describes in figure 3(b), when INPUT goes to GND from VDDL during HIGH state of HD_EN signal, N1 and N2 are turned off but P0 is turned on. Therefore, node D becomes VDDL-Vth+α by the capacitance coupling effect of node B which is charged to VDDL, where α is VDDL·C0/(C0+C_{par}), 0.8VDDL, and C_{par} is parasitic capacitance of node D. Now, when P1 is turned on by the voltage of node D, node C becomes HIGH by charge sharing, OUTPUT discharges to GND because N3 is turned on. Finally, when HD_EN becomes LOW signal, LOW state is stored, because node A and OUTPUT are connected by N4.

3. Simulation Results

The system specification is summarized in Table 1. The proposed circuit is verified by the HSPICE with the RPI level 62 for LTPS. The output load is 50fF for gate capacitance of a CMOS inverter. We assume that the system has 6-bit color depth and source driver output has channels as number of pixels by 1:3 de-multiplexing to sub-pixel. The power supply voltage is determined by DAC for level shifting from 5V to 7V.

Table 1. System Specification

Depth of color	6-bit
De-multiplexing	1:3 De-multiplexing
VDDL	5V
VDDH	7V
Input swing range	0~5V
Output swing range	0~7V

Figure 4 is the HSPICE simulation results of the proposed circuit in 62.5 kHz of operation frequency for qVGA resolution. As explained about operation above, if HIGH state is inputted while HD_EN signal is HIGH in T1, node A becomes VDDL and node D becomes VDDL-Vth, then OUTPUT is charged to VDDH. When LOW state is inputted in T2, node C and D is charged to high voltage about 8V by capacitance coupling, OUTPUT is discharged to GND.

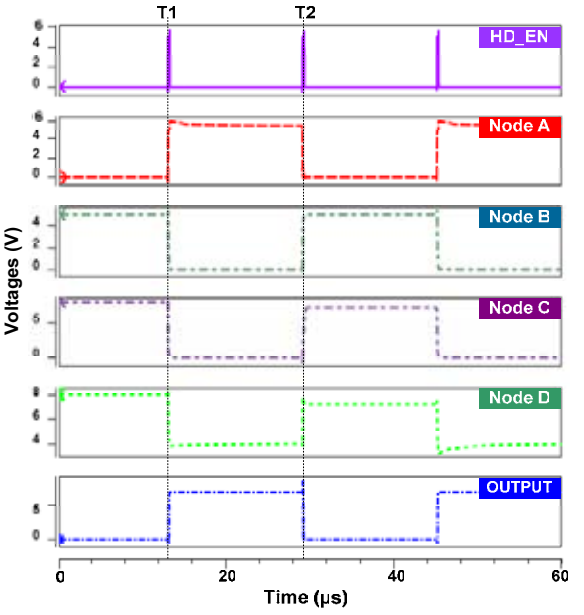


Figure 4. Simulation waveforms of proposed circuit.

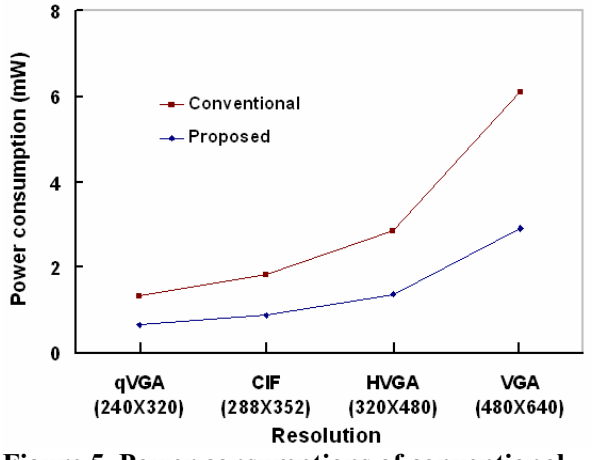


Figure 5. Power consumptions of conventional and proposed circuits.

The Simulation results of power consumption according to resolution are shown in Figure 5. Power consumption of the proposed circuit is less than 50% compared with conventional circuits. Therefore the proposed circuit is suitable for mobile applications.

4. Measured Results

To verify and compare performance of the proposed circuits with the conventional, we implemented both circuits. Figure 6 shows microphotographs of the fabricated circuits on glass substrate which are layout of a conventional structure and the proposed circuits according to 2.2inch qVGA resolution with 5μm design rule. As mentioned above, the panel system uses 1:3 de-multiplexing and 3 sub-pixels have only 6-bit latches per channel. The pixel pitch of 2.2-inch qVGA is 139.5μm, thus 18-bit of RGB data is integrated in 418.5μm. In same width, heights of the conventional and the proposed circuits are 1,217μm and 1,087μm, respectively, and the layout area is decreased by 10%.

Figure 7 is the measured results of the proposed circuit. Even if the INPUT changes, the OUTPUT is only changed when the HD_EN signal is HIGH state and range of OUTPUT swing voltage increase. Therefore, we can confirm that proposed circuit has both functions of a holding latch and a level shifter.

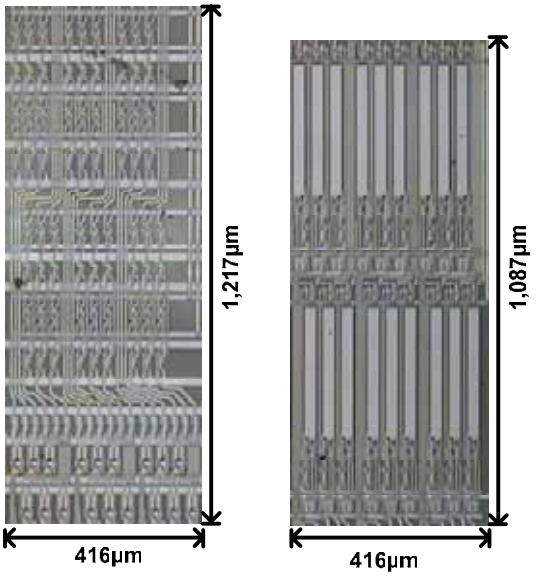


Figure 6. Microphotographs of fabricated circuits (a) conventional structure, (b)proposed circuit.

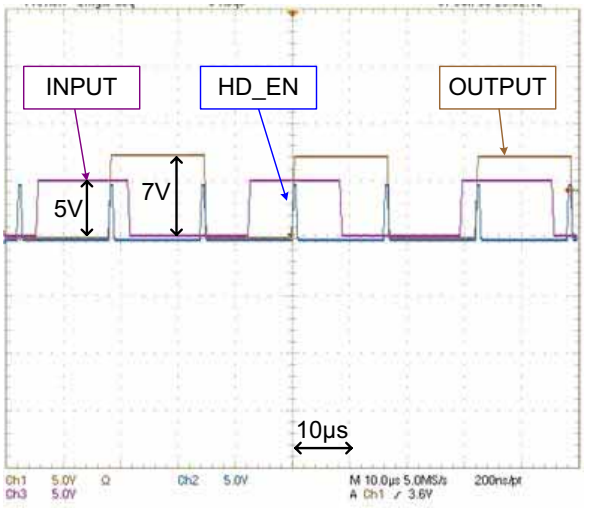


Figure 7. Measured waveforms of proposed circuits.

5. Conclusion

The simulation results verify the operation of the proposed circuit. Power consumption and layout area of the circuit is 50% and 90% of those of the conventional structure, respectively. The measurement result of the fabricated confirms the function of the proposed circuit.

Especially, the circuit is suitable for low-power system because it consumes only 75% of power of the typical structure [2].

6. Acknowledgements

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7. References

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