Data identified Time Extension Driving Method

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Abstract
A new liquid crystal display (LCD) Data identified Time Extension (DiTEX) driving scheme with a high charged voltage is proposed. The different charged voltage owing to the differential charging time and various initial pixel-potential can be eliminated or diminished under this method. It is compatible with a 2-row inversion and can be realized into the commercial dual-sided gate circuits.

1. Introduction
Nowadays, interpolated frame has been inserted into the middle of two normal video frames in order to depress the blurring effects caused by the hold-time type of displays. It effectively improves the image quality of motion pictures in LCDs and it will become a popular method in the display marketing soon later. However, the function of 120Hz frame rate is required to design into LCD applications [1]. Therefore, the insufficient charging time will be the significant problem in the high resolution of LCDs and in the fast frame rate of LCDs. Previous studies such as, Dual-Pulse driving method [2] and Line Time Extension (LiTEX) driving method [3] were expected to enhance the charged voltage from some line else. Both of them seemed to increase the charged voltage, but an inconsistent voltage would be obtained even if the input data is the same in several cases. It causes poor image qualities. In this paper, these worse cases will be simulated. Then, the novel DiTEX is capable of the image quality improvements. So, DiTEX is found that it not only greatly increases the charged voltage, but also resolves the pseudo-horizontal line effect [4].

2. Prior Driving Methods
Previous driving methods can be simulated by the same conditions of the supposed SPICE model which is based on the circuits of Figure 1 and the parameters of Table 1. All of the parameters have been assumed to be close as the physical values as possible.

2.1 Traditional Progressive Single Line (TPSL) Driving Method
TPSL is very common in marketing because of simplicity. However, when it is applied to high definition and high aperture ratio of LCD applications, the charged voltage of TPSL is critical. Hence, the performance of TPSL is prepared to evaluate again. There is an extreme condition which is interested to us. First of all, the normally white pixel is turned on to be the black in the negative frame. After the line inversion, the pixel is still held on the black in the positive frame. Simulated data is shown as Table 2, the pixel-voltage is charged to 9.45V from original -0.64V. The compared case is that the pixel is turned on to be the white in the negative frame. After the line inversion, the pixel is transferred to the black in the positive frame. The pixel-voltage is changed to 9.56V from initial voltage of 4.10V. To analyze this case, the pixel has a different final charged voltage even if the present data is the same. According to this situation, the differential final charged voltage is claimed as the variation voltage ($\triangle$V). When the motion pictures are playing, this factor contributes to the order of dynamic contrast ratio variation. In the other words, regarding the maximum high charged voltage in the table, it is insufficient value apparently.

2.2 Dual-Pulse Driving Method

The next two compensated driving methods are Dual-Pulse driving method and LiTEX driving method. In the Dual-Pulse mode, the transition of the pixel-voltage from $0V_{N+2(t-1)}$ to $10V_{N+2(t)}$ is no longer existed and is replaced by the curve from $5V_{N+2(t-1)}$ to $10V_{N+2(t)}$. The maximum high charged voltage is optimized to $9.92V_{N+2(t)}$ based on the source voltage curve from $5V_{N(t-1)}$, $10V_{N(t)}$ to $10V_{N+2(t)}$ which is different from that the maximum high charged voltage is $9.56V_{N+2(t)}$ based on the source voltage curve from $5V_{N(t-1)}$, $5V_{N(t)}$ to $10V_{N+2(t)}$. The previous data is $D_{N+2}(t-1)$ in the $N+2_{th}$ line is modified to the other value of the present data $D_{N+2}(t)$, but the final present charged voltage $V_{N+2}(t)$ come out two possible results of the maximum high charged voltages as Table 2. The differential maximum high charged voltage is defined as the variance voltage (dV). It is because the previous data $D_N(t-1)$ of the N_{th} line is different from the present data $D_N(t)$ of the N_{th} line. The value of dV brings the pseudo-horizontal line during playing the static picture.

2.3 Line Time Extension (LiTEX) Driving Method

The LiTEX mode is relied on the 2-line inversion (2H1V) [3] different from the dot inversion. The 2H1V Inversion mechanism is able to provide the acceptable image qualities in various applications. About the scheme of the LiTEX, the first step is required to search for an optimal time extension (t_{EXT}) depended on a special condition. The special condition is needed to be satisfied that the maximum high charged voltage $V_N(t)$ of the N_{th} line based on the source data curve from 0V to 10V is asked to equal to the maximum high charged voltage $V_{N+1}(t)$ of the $N+1_{th}$ line based on the source data curve from 0V, 5V to 10V. Through the many trials, the t_{EXT} is found. The final t_{EXT} is calculated about 1.5us and the identical maximum high charged voltage is about 9.51V in accordance with the same previous assumed circuit and parameters.

3. Results

According to the conceptions of D. A. Fish [5] and L. Lin [6], the charging time taken is more than discharging time taken in TFT LCD, which has been proved by the equations shown as below.

$$V_n = V_{no} \quad at \quad t = 0 \qquad \text{.....(1)}$$

$$V_n = \frac{1 - a \ \exp(-t/\tau)}{1 - b \ \exp(-t/\tau)} V_d \qquad \text{.....(2)}$$

$$\tau = \frac{C_{px}}{\beta_0 (V_g - V_t - V_d)} \qquad \text{.....(3)}$$

$$a = \frac{V_d - V_{no}}{V_d} \frac{2(V_g - V_t - V_d) + V_d}{2(V_g - V_t - V_d) + V_d - V_{no}} V_d \qquad \text{..(4)}$$

$$b = \frac{V_d - V_{no}}{2(V_g - V_t - V_d) + V_d - V_{no}} \qquad \text{.....(5)}$$

The node potential V_n represents the potential of the pixel electrode. The initial value V_{no} is defined as the node potential at the leading edge of a gate pulse. The gate-on voltage is V_g. The threshold voltage of the TFT is V_t. The drain voltage is V_d. The gate-on effective time is t, and τ stands for a time constant defined by equation (3). In the equation (3), β_0 is decided by the mechanical factor and the equation is expressed as below.

$$\beta_0 = \mu_n C_i (W / L) \qquad \text{.....(6)}$$

Where μ_n is the electron mobility in the a-Si channel, Ci is the gate insulator capacitance per unit area, and W and L are the width and length of TFT structure respectively. The factor C_{px} is equal to $C_{lc}+C_{st}+C_{gs}$. In the equation, the parasitic capacitance between gate and the source is C_{gs} , C_{lc} is the capacitance of liquid crystal, and C_{gs} is the capacitance of storage capacitance.

The novel driving method is originated from the same ideal that the discrepant charging and discharging time exists in the dynamic behavior of TFT displays. This conception has been simulated on Figure 2. The curve –g– is assumed that the pixel voltage data is transferred from 0V to 10V. The charging time is about 52.6us, when the charged voltage is 9.90V. The curve –h– is assumed that the pixel voltage data is transferred from 0V to 5V. Its charged is about 15.4us, when the charged voltage is 4.90V. The curve –i– is assumed that the pixel voltage data is transferred from 0V to 0V. Its charged is about 3.2us, when the charged voltage is 0.09V due to the couple voltage from leading edge of gate signal. The VGS is larger, the charging or discharging time is less. Usually, the VGS- is larger in the negative polarity

than the VGS+ in positive polarity. According to the feature as well as a special algorithm, the charging time can be expanded by shrinking the discharging time. The novel DiTEX driving scheme is deduced by the general circuitry model of Table 1 under the condition of the 2H1V inversion type. It is quite simple to take the additional period t_{EXT} in DiTEX. In the beginning, the optimal row scan time is defined by the discharging time (T_n), which is the transition period of from the maximum high pixel voltage to discharge to middle voltage V_M. Subtract the two times of T_n from the two times of traditional row scan time of TPSL. Hence, the amount of t_{EXT} is easily to be calculated. If there is a shorter T_n, t_{EXT} can be extended longer. At last, DiTEX is necessary to identify the maximum value between the sharing coupled lines. The equation is revealed as below.

$$D_{MAX[N,N+1]} = Max[D_N, D_{N+1}] \quad (1.)$$

Where D_{MAX}, D_N, D_{N+1} stand for the identified maximum value, the data of N row, and the data of N+1 row respectively. Put this identified maximum value to the period of t_{EXT}, but keep the two rows raw data in original individual two T_ns. The equations are shown as below.

$$\text{Row N}: \ [t_{EXT}: T_1], \ \Rightarrow [D_{MAX[N,N+1]}: D_N], \quad (2.)$$

Row N+1:$[t_{EXT}: : T_2]$,$\Rightarrow[D_{MAX[N,N+1]}: : D_{N+1}]$, and so on.

Where t_{EXT}, T_1 and T_2 stand for extension time and two T_ns period time. The driving waveform illustration is shown on Figure 3 and the simulation is shown as Figure 4.

4. Conclusions

The △V of DiTEX equals zero as Table 2. The null amount is the same as the value of TPSL. It means that the driving method enables the dynamic contrast ratio without any variation when the motion pictures are playing. The dV of DiTEX is the least value equal to 0.08V which is allowed the free pseudo-horizontal line effects. Furthermore, the DiTEX promises a high charged voltage. The DiTEX makes the min.(max.) high voltage equal to 9.57V (9.65V). It is more than the min. (max.) high voltage of TPSL which is equal to 9.45V (9.56V). For the time extension, the row time of DiTEX not only upgrades to 29.5us compared to 26us of TPSL, but also improves t_{EXT} to 7us compared to 1.5us of LiTEX. Nevertheless, the four driving methods have the small residual discharged voltage, but they do not impact the performance as much owing to the normal white panel. DiTEX is also useful for common AC signal situations, so it is applicable to mobile applications especially for dual-sided embedded gate panels [7]. Therefore, the novel DiTEX promises a high charged voltage, is able to expand the charge time, provides a free pseudo-horizontal line effect and is effectively to improve the dynamic and static image qualities.

5. Acknowledgements

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6. References

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Circuitry	3Row*2Column Cell Matrix
TFT	Model= 35, W/L= 12um/4um, C_{gd}= 1.53E-15 farad, C_{gs}= 3.02E-15 farad
LC	R_{LC}= 1E12 Ohm, C_{LC}= 1.64E-14 farad
Storage Cap.	C_{ST}=1.956E-13 farad
Cross Cap.	$C_{Scan-Data}$= 4.57E-15 farad, $C_{Com-Data}$= 3.26E-15 farad
Resistance	$R_{Metal-I}$= 14.59, $R_{Metal-II}$= 5.32, $R_{Com-ITO}$= 5.32, $R_{Pixel-ITO}$= 21.89

(Unit: Resistance= Ohm/□)

Table 1. Simulation circuitry parameters

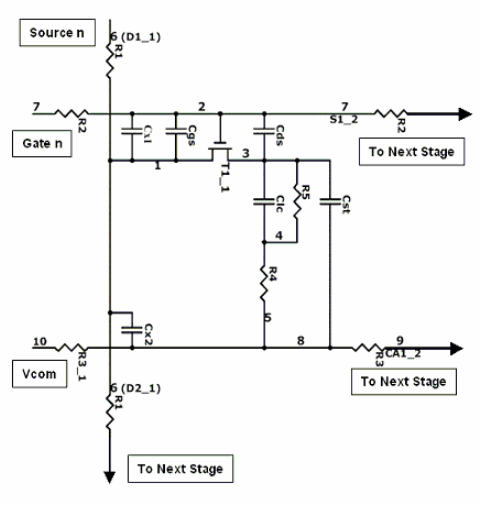
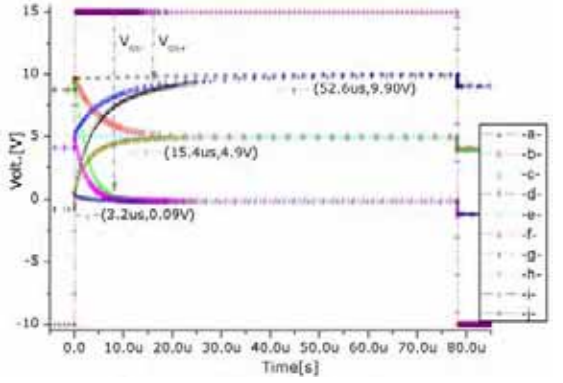


Figure 1. Simulation circuits.



- **g** - Data from D_N(t-1) =0V to D_N(t)=10V
- **h** - Data from D_N(t-1) =0V to D_N(t)=5V
- **i** - Data from D_N(t-1) =0V to D_N(t)=0V;

Figure 2. TFT (W/L=12um/4um) charged & discharged curve

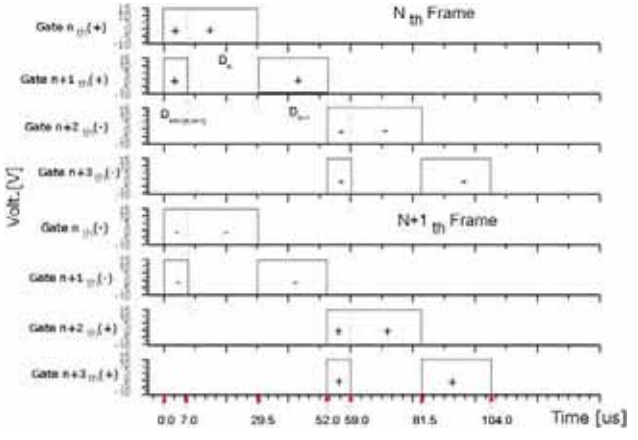
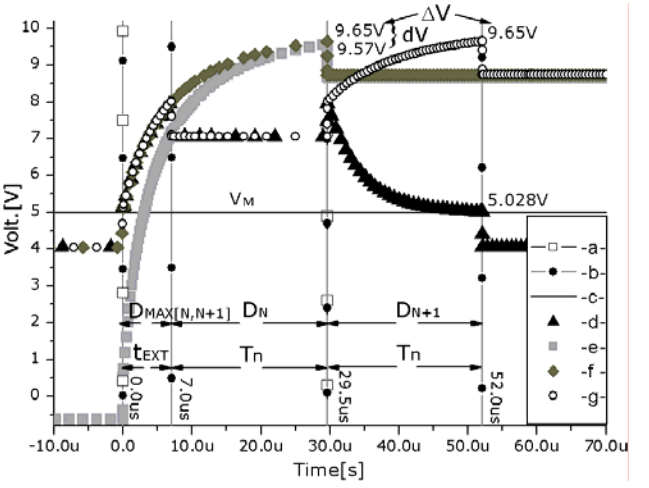


Figure 3. Conception of DiTEX waveform diagram



- **a** - The N^{th} row gate signal: V_{GH}=15V, V_{GL}=-10V; from 0.0us to 29.5us
- **b** - The $N+1^{th}$ row gate signal: V_{GH}= 15V,V_{GL}=-10V; from 0.0us to 7us & 29.5us to 52us
- **c** - Middle voltage V_M=5.0V
- **d** - V_{N+1}(t) =5.028V; from D_{N+1}(t-1)= 5V to $D_{MAX[N,N+1]}$ =10V to discharge to V_M
- **e** - V_N(t)=9.57V; from D_N(t-1)=0V to $D_{MAX[N,N+1]}$ =10V to D_N(t)=10V
- **f** - V_N(t)=9.65V; from D_N(t-1) =5V to $D_{MAX[N,N+1]}$ =10V to D_N(t)=10V
- **g** - V_{N+1}(t)=9.65V; from D_{N+1}(t-1)=5V to $D_{MAX[N,N+1]}$ =10V to D_{N+1}(t)=10V

Figure 4. The novel DiTEX Driving waveforms

	D_N(t-1)	$D_{MAX[N,N+1]}$	D_N(t)	D_{N+1}(t)	D_{N+2}(t)	V_N(t-1)	V_N(t)	V_{N+1}(t)	V_{N+2}(t)	△V	dV
TPSL	0		10			-0.64	9.45			0.00	
	5		10			4.10	9.56			0.00	
Dual-Pulse	0		10		10	-0.63	9.45		9.89	0.44	
	5		10		10	4.08	9.56		9.92	0.36	
LiTEX	0		10	10		-0.65	9.51	9.90		0.39	
	5		10	10		4.10	9.61	9.91		0.30	
DiTEX	0	10	10	10		-0.64	9.57	9.57		0.00	
	5	10	10	10		4.06	9.65	9.65		0.00	
TPSL	0		10			-0.64	9.45				0.11
	5		10			4.10	9.56				
Dual-Pulse	0		5		10	-0.63	4.99		9.56		0.36
	0		10		10	-0.63	9.45		9.89		
	5		5		10	4.08	4.99		9.56		
	5		10		10	4.08	9.56		9.92		
LiTEX	0		5	10		-0.64	5.00	9.51			0.4
	0		10	10		-0.65	9.51	9.90			
	5		5	10		4.10	5.00	9.51			
	5		10	10		4.10	9.61	9.91			
DiTEX	0	10	10	10		-0.64	9.57	9.57			0.08
	0	10	5	10		-0.64	5.02	9.57			
	5	10	10	10		4.06	9.65	9.65			

(Unit: Voltage)

Table 2. The comparisons of △V and dV for four driving methods