The effect of 3-mercapto-5-nitro-benzimidazole (MNB) and poly (methyl methacrylate) (PMMA) treatment sequence organic thin film transistor

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Abstract

A bottom contact organic thin film transistor (OTFT) is fabricated with an organic double-layered gate insulator (GI) and pentacene. The PMMA and MNB layers are treated on gate insulator and source/drain (S/D, Au) before depositing pentacene to investigate device properties and pentacene growth. The sequence of surface treatment affects a device performance seriously. The ultra-thin PMMA (below 50A) was deposited on organic gate insulator and S/D metal by spin coating method, which showed no deterioration of on-state current (Ion) although bottom contact structure was exploited. We proposed that the reason of no contact resistance (Rc) increase may be due to a wettability difference in between PMMA / Au and PMMA / organic GI. As a result, the device treated by PMMA → MNB showed much better Ion behavior than those fabricated by MNB → PMMA. We will report the important physical and electrical performance difference associated with surface treatment sequence.

1. INTRODUCTION

Organic thin film transistors (OTFTs) have gained great interests due to their unique properties exhibited by organic semiconductors. However, the limitation to a larger exploitation of organic TFTs comes from their low mobility, which is, at best, two or three orders of magnitude lower than that of conventional silicon. Another obstacle towards a larger development and utilization of organic materials is the poor knowledge of the microscopic charge transport processes, the nature of the metal interface, and the degradation mechanisms that affect the device performance.

Nevertheless, impressive progress has been made towards the final goal of realizing reliable electronic performance in realistic applications such as flat panel display, radio frequency identification tag (RFID), sensors, etc. for a last decade [1-5].

However, nobody has commented about the limitation of mobility and on current / off current modulation (Ion/Ioff ratio). Thus, many researchers have selected their development targets similar to those of a-Si TFT. In most case, the mobility level and Ion/Ioff ratio of a-Si TFTs are ~ 0.5 cm^2/Vs and 10^6 - 10^7, respectively. Recently, the mobility of OTFTs is improved even more than 0.5 cm^2/Vs, thus, it's not a big issue any more (3 - 5 cm^2/Vs can easily be obtained from the pentacene TFT) [6]. But, the off current control has still been very problematic due to a difficulty of interface control during evaporation and patterning of organic semiconductor.

The increase of off current level of OTFTs can be resulted from the following reasons: 1) the leakage current through the gate insulator (vertical leakage) and 2) the leakage current through the interface in between active channel and gate insulator (peripheral leakage).

The second problematic issue could be solved by the patterning of active layer. But, the source of peripheral leakage could also results in the Vth variation, hysteresis, etc. Thus, the origin of this phenomenon should be removed from the device.

For this purpose, we have developed a very unique and simple procedure by introduction of very thin PMMA layer. From this technology we successfully suppress the off current level below 10^{-11} A and obtained very low hysteresis with no increase of contact resistance.

2. DEVICE FABRICATION

In this paper, we fabricated pentacene TFT with bottom gate and bottom contact structure, as illustrated in Fig. 1. MoW was deposited and patterned on glass substrate as a gate electrode (2000 Å). Then, A BCB (3000 Å) and S4 (3000 Å) was successively spin casted as a gate dielectric layer. The Au (S/D electrodes) was deposited by thermal evaporator ~ 700 Å by using SUS open mask. And the surface of Au and GI was treated by PMMA and MNB (or MNB and PMMA), successively. Finally, the 600 Å pentacene layer was also deposited on the treated surface by same method (substrate temperature during vacuum evaporation: 80 ℃, deposition rate of 0.5 Å/s).

The device properties were evaluated by Keithley 4200, gate sweep range was from +40 V to 40 V with 0.5 V step. Current-voltage curves were measured at –20 V. The TFT size was 1000 um/100 um.

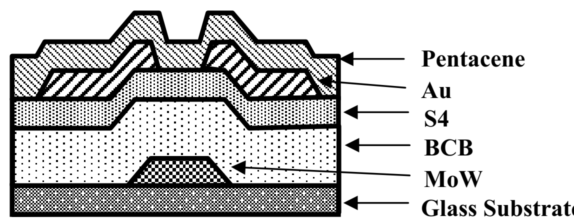

Fig. 1. Cross sectional view of bottom contact pentacene TFT structure.

3. RESULTS AND DISCUSSION

Fig 2 shows the output characteristics of OTFTs obtained by different surface treatment condition. PMMA layer was introduced to improve the interface of S4 – pentacene and MNB was treated to reduce a contact resistance at Au – pentacene interface. In this case, the sequence of surface treatment affects the device performance very differently because polymer solution could normally be covered all the area including Au and GI surfaces. Thus, we reduce the thickness of PMMA below 50 Å to achieve the tunneling effect at contact area. In addition, we split the sequence of PMMA and MNB treatment. Fig 2(a) shows the output curve of OTFT device treated by an order of PMMA → MNB. Fig 2(b) was then obtained from the reverse condition (MNB → PMMA). Very interestingly, we obtained very good contact behavior when we treated the surface by PMMA → MNB although MNB → PMMA gives the much lower Ion level as well as much worse contact behavior.

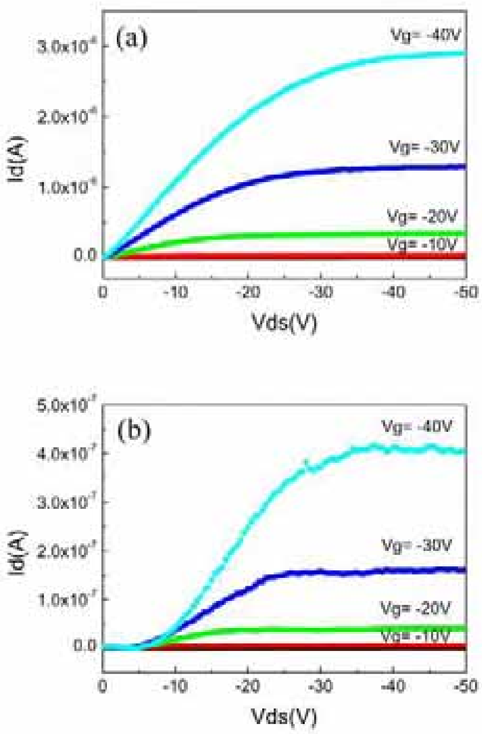

Fig 2. The output curves of the OTFTs which treated by: (a) PMMA → MNB, and (b) MNB → PMMA, respectively.

To investigate a surface morphology after treatment of PMMA, we blended a small amount of fluorescent polymer into PMMA solution (100 : 5 = PMMA : green-PPV, vol./vol.). When we spin casted a PMMA solution by 200 Å thick, we found that extensive area of Au was also covered by polymer. [See Fig 2(a), the dark area is the surface of Au. From the dark area, we could find many fluorescent spots which indicate the polymer residue.] However, the amount of polymer residue is seriously reduced if we control the thickness below 100 Å.

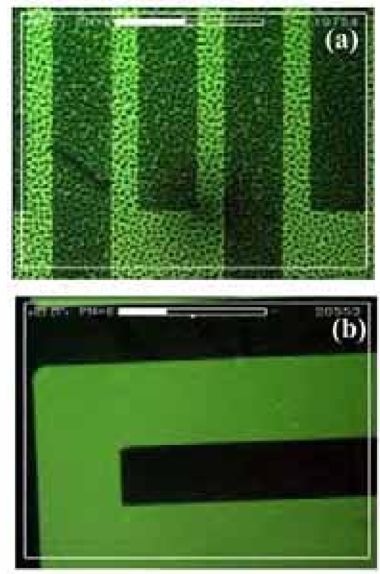

Fig 2. The fluorescent microscopic images of PMMA blended by adding of fluorescent material (FM) (PMMA:FM = 20:1): Total Thickness: (a) 200 Å and (b) < 100 Å, respectively. The surface of GI was spin casted by ~ 50 Å of PMMA for the actual devices tested in this paper .

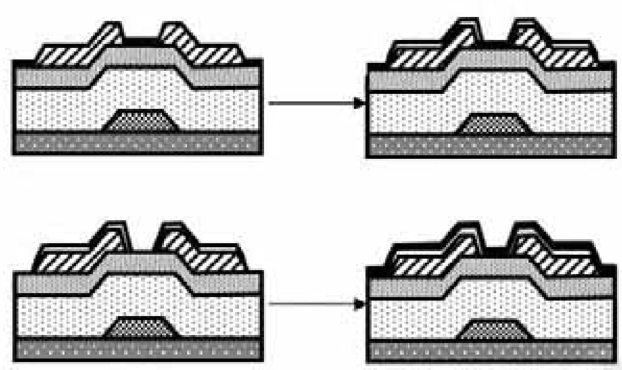

Fig 3. The surface treatment of OTFT devices: (a) PMMA followed by MNB, and (b) MNB followed by PMMA, respectively.

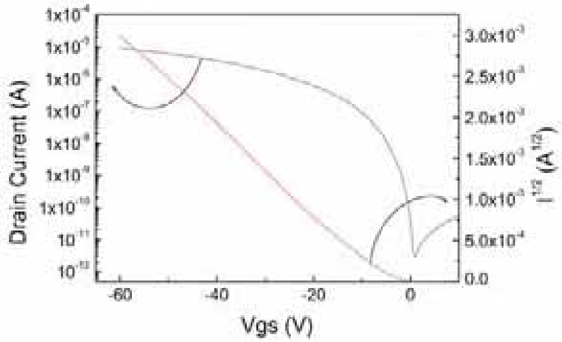

Fig 4. The surface treatment of OTFT devices: (a) PMMA followed by MNB, and (b) MNB followed by PMMA, respectively.

Figure 4 is a plot of drain current versus gate–source voltage at drain–source voltage of -35 V, from which, TFT characteristics can be extracted: the saturation field-effect mobility is 0.3 cm V s, the threshold voltage is about -2.0 V, and on/off ratio is greater than 10^5.

4. CONCLUSION

We showed that off current level was dramatically reduced by laser patterning technique without any on current drop of pentacene TFT device. Resultantly, the pentacene TFT we tried in this paper showed off current level about 10^{-9} A which is improved by 2 - 3 orders of magnitude after pentacene patterning compared to that of non-patterned device. Using such pentacene TFT, we successfully demonstrated 1.5 inch EPD display.

5. ACKNOWLEDGMENT

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