The Dependence of Mechanical Strain on a-Si:H TFTs and Metal Connection Fabricated on Flexible Substrate

M. H. Lee*, K.-Y. Ho, P.-C. Chen, C.-C. Cheng, and Y.-H. Yeh
Display Technology Center, Industrial Technology Research Institute (DTC/ITRI),
Hsinchu, Taiwan

*Phone:+886-3-5912337, E-mail: <u>MinHungLee@itri.org.tw</u>

Abstract

We evaluated a-Si:H TFTs fabricated on polyimide substrate (PI) at the highest temperature of 160 °C with uniaxial and tensile strain to imitate flexible display. With tensile strain, the threshold voltage of a-Si:H TFTs have positive shift due to extra dangling bond formation in a-Si:H layer. However, no significant degradation of the subthreshold swing and effective mobility with tensile strain of a-Si:H TFTs indicates the similar level of band tail state. The metal wire with the width of 10 µm for connection on flexible substrate can sustain with curvature radius 2.5 cm.

1. Introduction

Lightweight, toughness, flexibility, and unrestrained design make the electronics on plastic substrates attractive on many applications like portable instruments, e-paper, RFID, and PDA [1]. However, there are many challenges for TFTs fabrication on flexible substrate due to higher coefficient of thermal expansion (CTE) and lower glass transition temperature (T_o) as compared with the electronics on glass substrate prevent plastic substrate deformation and damage, the TFTs fabrication process is required as low temperature as possible. Due to less period of crystal structure in amorphous silicon, the carrier mechanism with strain is dominated by trapping and de-trapping in a-Si:H TFTs [3]. Unlike the energy band deformation and effective mass reduced in crystalline Si FETs of CMOS [4], the performance of a-Si:H **TFTs** exhibits substantially less enhancement [5] with uniaxial and tensile strain. In this study, we will apply the strain smaller than 0.3% to ensure a-Si:H TFTs not to fail [4]. The electrical characteristics of aSi:H TFTs on curved surface need to consider as simulation and design for the flexible display.

2. Device Fabrication

An 18 cm x 18 cm polyimide (PI) substrate was used as a flexible backplane with the thickness of 40 um. A 200 nm SiO_x layer was deposited as a buffer layer to prevent the moisture and solvents permeating into the film while increasing the adhesion to the TFT layers [6]. An inverted staggered back-channel etched (BCE) a-Si:H TFT was fabricated on the PI substrate as shown in Fig. 1 & 2. The gate metal line is Ti/Al/Ti with the total thickness of 200 nm, and deposited by DC sputtering system. The conventional structure of BCE a-Si:H TFTs was used with 50 nm n⁺-a-Si:H / 200 nm a-Si:H / 300 nm a-SiN_x:H layers deposited by PECVD at the substrate temperature of 160°C. Island region and contact holes are patterned and defined by photo-lithography and following dry etching

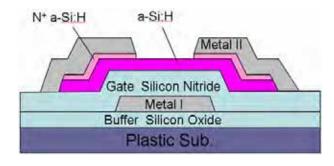


Fig. 1. The schematic diagram of The BCE a-Si:H TFTs backplane. The structure of BCE a-Si:H TFTs was used with 50nm $\rm n^+$ -a-Si:H/200nm a-Si:H/300nm a-SiN_x:H layers deposited by PECVD at the substrate temperature of 160° C.



Fig. 2. The a-Si:H TFTs backplane are bonding on camber chuck and vacuumed to fix for electrical measurement. There are three camber chucks with curvature radius 10 cm, 5 cm, and 2.5 cm were used to apply the mechanical strain.

processes. Finally, 200 nm Ti/Al/Ti layer was deposited by DC sputtering and then patterned for the source/drain electrode by dry etching process.

3. Results and Discussion

Three camber chucks with curvature radius 10 cm, 5 cm, and 2.5 cm were used to apply the mechanical strain on the TFTs and the effective strains were 0.05%, 0.1%, and 0.2%, respectively. There were five kinds of metal wire layout with the width of 10 µm, which can be the scan lines or data lines in the TFT array, for the reliability analysis of mechanical strain. The structures included: (1) single metal layer: straight (Fig. 3(a)), saw (Fig. 3(b)) and step (Fig. 3(c)), and (2) double metal layer: finite-segment connection through contact holes (Fig. 3(d)) and double layer connection through contact holes (Fig. 3(e)). No resistance degradation was observed with tensile strain ~0.2%, and no broken wires occurred after over 5000 times bending stress as shown in Fig. 4. This phenomenon indicated the electrical

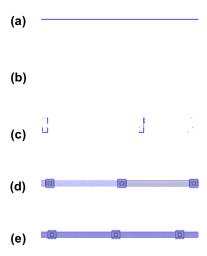


Fig. 3. Five kinds of metal wire layout with the width $10~\mu m$: (a) straight, (b) saw, (c) step, (d) finite-segment connection through contact holes, and (e) double layer connection through contact holes.

characteristics of a-Si:H TFTs was independent of the parasitic effect from the metal wire under mechanical strain. The straight metal line can sustain to flex more than 5000 times with minimum curvature radius 2.5 cm (strain=0.2%). The threshold voltage of a-Si:H TFTs shifted to positive, which is observed from the transfer characteristics while strain increasing as shown in Fig. 5. The similar trend was obtained from the shift of capacitance at 900 Hz, which is low enough for carrier response in a-Si:H layer as shown in Fig. 6. The shifts of threshold voltage and capacitance showed the dangling bond induced in a-Si:H layer while strain increasing, and higher gate bias can compensate the traps for channel formation. The longer duration time in C-V and/or possible fix trap formation in SiN_x with strain increasing caused larger capacitance shift. The effective mobility of a-Si:H TFTs with strain had slightly higher than that of original TFTs (w/o strain), and subthreshold swing had no apparent variation. This presented the generation of band tail state of a-Si:H layer was not significant while strain increasing. Note that the

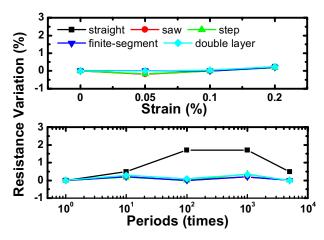


Fig. 4. The variation of metal wire resistance under mechanical strain and bending stress. No resistance degradation was observed under mechanical strain $\sim 1.5\%$ and kept continuity after more than 5000 times bending stress.

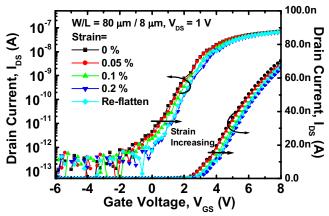


Fig. 5. The transfer characteristics of a-Si:H TFTs backplane on plastic substrate with different strain. The W/L of all TFTs is 80 μ m/8 μ m. Note that smaller devices have more random trend of threshold voltage shift (not shown in the figure).

induced dangling bond can not be recovered "immediately" after the strain releasing (reflatten) to virgin devices (1st bending), and it caused the threshold voltage and capacitance shifts not return to original condition as shown in Fig. 7.

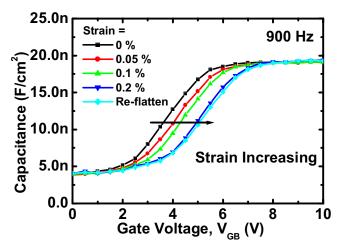


Fig. 6. The capacitance–voltage of a-Si:H TFTs backplane on plastic substrate with different strain at 900 Hz. The MIS area is $46 \mu m \times 67 \mu m$.

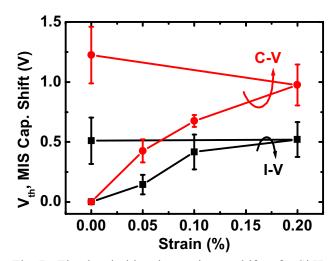


Fig. 7. The threshold and capacitance shifts of a-Si:H TFTs backplane on plastic substrate with strain increasing and releasing.

4. Summary

The BCE a-Si:H TFTs were fabricated on plastic substrate with the highest process temperature of 160°C. The metal wire can sustain the strain up to 0.2% and over 5000 times mechanical stress. The extra dangling bond, induced in a-Si:H layer while strain increasing, caused the shifts of

threshold voltage and capacitance. The electrical characteristics of a-Si:H TFTs under mechanical strain are useful for both simulation and design for the flexible display.

5. Acknowledgements

The authors are very grateful the fund support by Ministry of Economic Affairs & ITRI, Taiwan.

6. References

- [1] Beng Ong, "Ubiquitous Flexible Electronics," USDC, Sec. 1.2, 2006
- [2] G. P. Crawford, "Flexible Flat Panel Display," John Wiley & Sons, England, 2005.
- [3] Y. Kuo, "Thin Film Transistors: Materials and Processes Vol.1 Amporphous Silicon Thin Film," Kluwer Academic, MA, 2004.

- [4] M. H. Lee, P. S. Chen, W.-C. Hua, C.-Y. Yu, Y. T. Tseng, S. Maikap, Y. M. Hsu, C. W. Liua, S. C. Lu, W.-Y. Hsieh, and M.-J. Tsai, "Comprehensive Low-Frequency and RF Noise Characteristics in Strained-Si NMOSFETs," IEEE IEDM Tech. Dig., pp. 69-72, 2003.
- [5] H. Gleskova, S. Wagner, W. Soboyejo, and Z. Suo, "Electrical response of amorphous silicon thin-film transistors under mechanical strain," J. of Appl. Phys., vol. 92, pp. 6224-6229, 2002.
- [6] Chun-Cheng Cheng, Jung-Fang Chang, Yi-Hsun Huang, Yung-Fu Wu, Tung-Hui Yeh, "Integrated of Amorphous Si TFT and PDMLC Technology on Plastic Substrate," IDMC, p. 423-425, 2005.