High Speed Memory Module

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HIGH SPEED MEMORY MODULE DESIGN

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ADVANCED DESIGN TEAM
H.S.RYU

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INTRODUCTION

- According as the system operating frequency increasing rapidly, the high speed memory module is also needed.
- There are lots of consideration factors to minimize the noise due to the high speed operating.
- We should design the memory module to get the good signal integrity in consideration of the noise factors.

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HIGH SPEED MEMORY MODULE TREND

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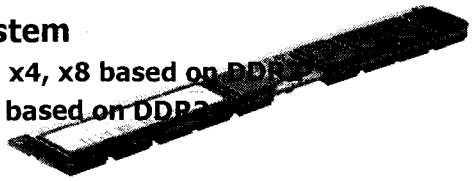
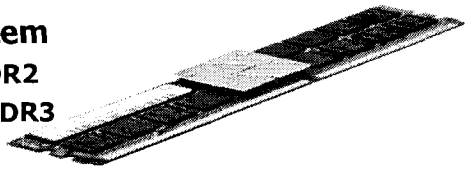
NEW MEMORY MODULE TYPE

- Desktop system
  - Unbuffered DIMM → x8 , x16 based on DDR2 and DDR3
- Laptop system
  - SODIMM → x8, x16 based on DDR2 and DDR3
- Low-end server system
  - Registered DIMM → x4, x8 based on DDR2
  - VLP DIMM → x4, x8 based on DDR2



- High-end server system
  - FBDIMM based on DDR2
  - FBDIMM2 based on DDR3



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MEMORY MODULE TREND

- Traditional Memory Module
  - Simplified Stack-up [4L/6L]
  - Single Z_0 control
  - Simple and Perfect referencing scheme.
- *New Structure due to the high speed memory module.*
  - Multi-layer (10 Layer ~)
  - Low power consumption
  - Multiple characteristic impedance control for the same signal.
  - Heat sink for thermal issue on the DIMM
  - Complex termination scheme to improve the signal integrity

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MEMORY MODULE TREND

- New Structure due to the high speed memory module.
  - Violence for the traditional referencing of the power distribution
  - Layer x-talk due to the thinner space between signal layers.

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DESIGN PROCESS

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Design Process

- Pre-simulation to find the solution which is satisfied with the SPEC.
  - Check the lots of feasibilities
  - Interface modeling
  - Make up the system assumptions
    - → Driver type & strength
    - → Loading condition
    - → Net Topology
    - → Target Z0
    - → Termination scheme
    - → Allowance the x-talk
    - → Referencing rule

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Design Process

- Design & Check
  - Design with assumptions from the pre-simulation
  - What is the mechanical problem?
- Post-simulation
  - Check the real design
  - Timing & voltage margin check
  - Revise the design file to improve the signal integrity
- Measurement
  - Function & application test
  - Feedback to design

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CONSIDERATION FACTORS

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How to improve the design?

- **Four ways to mitigate the impact of the reflection on the channel**
  - *Decreasing operating frequency*
  - *Simplified net topology*
  - *Short channel length compared to the wave length*
  - **Adequate termination scheme for each signal group**
- **Improve the off-chip PDN**
  - **Discontinuity factors – Socket/Package/Return Path**
  - **Decoupling capacitor optimizing**
- **Optimized consideration factors which are as follows.**

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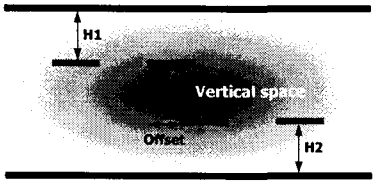
CONSIDERATION FACTORS

- **X-talk**
  - **Optimized connector pin assign with PWR/GND.**
  - **According as the vertical space closing up, x-talk between layers is serious compared to x-talk on the same layer.**
  - **This x-talk causes the impedance mismatch and impedance mismatch may cause noise.**
  - **To avoid coupling between Layers for the strip line.**



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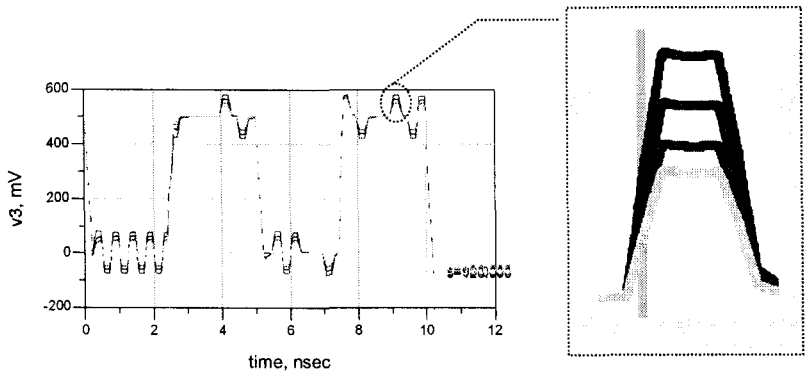
CONSIDERATION FACTORS

- **X-talk noise effect from the vertical space**
  - **→ Vertical space = 90, 120, 150, 180**
  - **→ Offset = 0**



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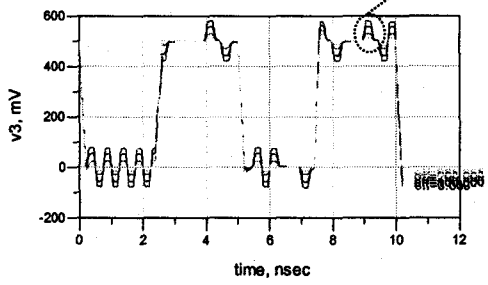
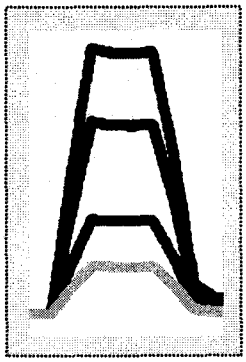
CONSIDERATION FACTORS

- X-talk noise effect from offset
  - → Vertical space = 90
  - → Offset = 0, 100, 200, 300
- According as offset increasing, x-talk noise is decreasing dramatically.





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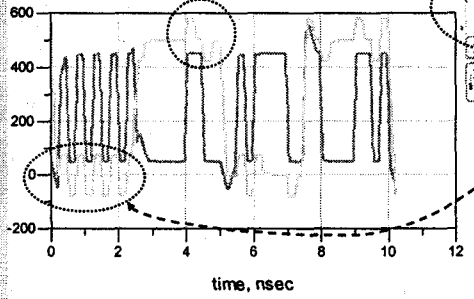
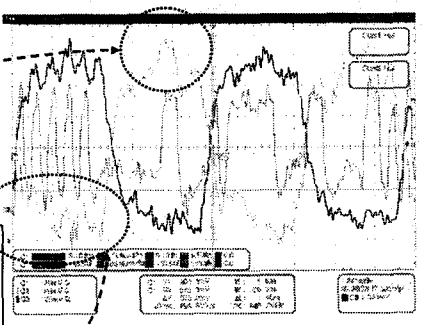
CONSIDERATION FACTORS

- Example waveform

Near-end Crosstalk waveform
Vertical space : 90 um
Offset = 0





We can see the near-end x-talk at the 90um vertical space and zero offset.

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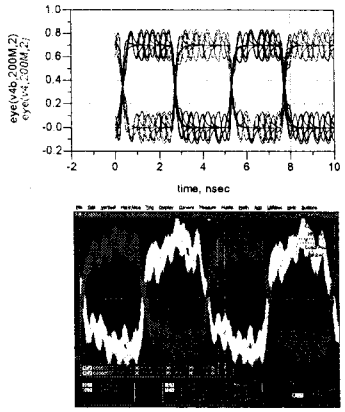
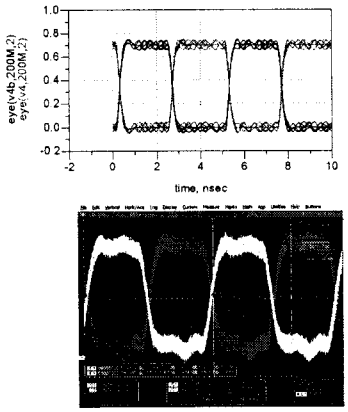
CONSIDERATION FACTORS

□ **Simulation Results – with Crosstalk vs. without x-talk**

Vertical space = 90
Offset = 0



Vertical space = 150
Offset = 200



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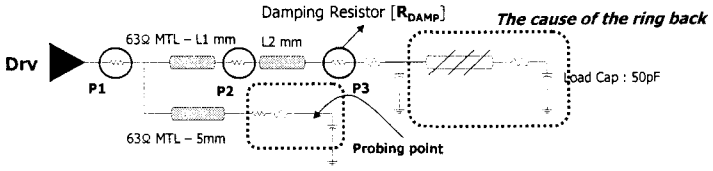
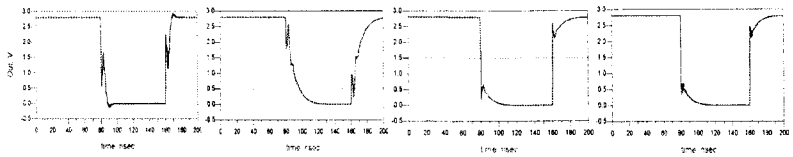
CONSIDERATION FACTORS

❑ **Termination method**





[No R_{DAMP}] [R_{DAMP}– P1] [R_{DAMP}– P2] [R_{DAMP}– P3]

□ **Signal integrity can be improved with the damping resistor.**

□ **Location of R_{DAMP} is also important.**

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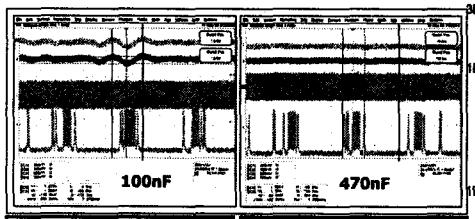
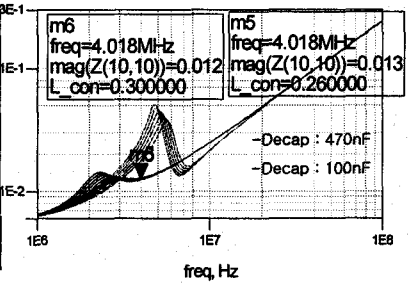
CONSIDERATION FACTORS

- **Off-chip PDN**
  - **Improving or shifting the resonance point to prevent from the noise at the specific frequency using the bulk capacitors and the decoupling capacitors.**



Failing	110mV/130ns	Failing	25mV/204ns
Rising	115mV/144ns	Rising	25mV/336ns



  - **Power noise is improved from changing the decoupling capacitor.**

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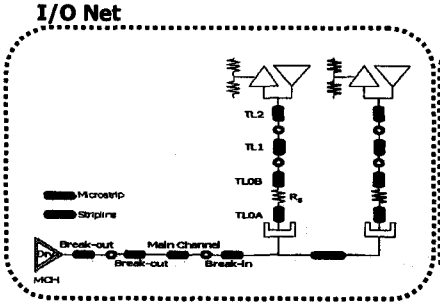
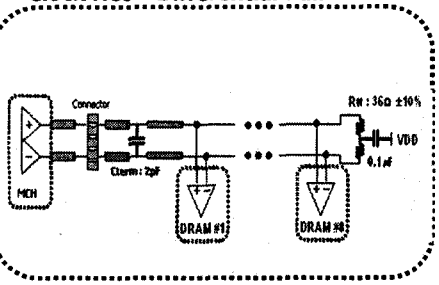
CONSIDERATION FACTORS

- **ISI (Inter symbol interference)**
  - **Impedance mismatching because of the channel topology**

I/O Net



Clock Net – Differential Pair



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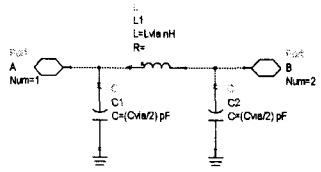
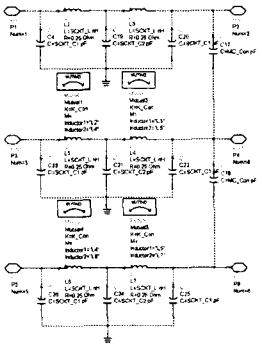
CONSIDERATION FACTORS

□ Discontinuity by the through via, the connector and the package.

→ Via Model



→ Socket Model



□ Stub length which causes the ring back is limited.

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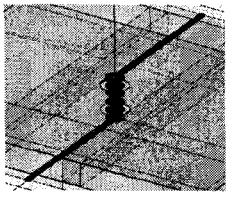
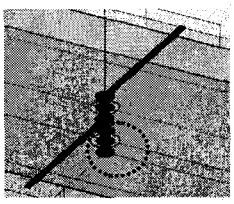
CONSIDERATION FACTORS

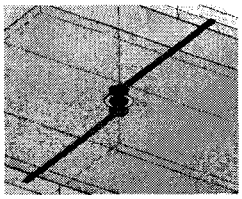
□ Using the blind Via instead of the through hole Via



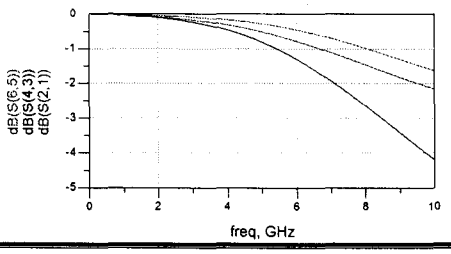
[Type 1]



[Type 2]



[Type 3]



→ *Via stub affects the signal transfer quality.*
→ *Via stub acts on the loss term*

Red : Type 1
Blue : Type 2
Pink : Type 3

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CONSIDERATION FACTORS

- Modeling Methodology for the accurate analysis
  - Lumped RLC model doesn't guarantee the accuracy at the high speed system.
  - S-parameter model from EM-simulation might be needed to analyze the channel interface.

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APPENDIX
[Design Example]

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Design Overview

- Module Configuration: 1Rank x8, Non-ECC
- Module Dimension: 67.60 X 30.00 mm
- Number of Layers: 8 Layer
- Maximum DRAM Size: 12.3 X 20 mm
- DRAM Pitch:
  - Between 1st and 2nd → 13.80 mm
  - Between 2nd and 3rd → 18.585 mm
  - Between 3rd and 4th → 13.80 mm
- Target Impedance
  - DQ/DQS/DM: 60 ohm
  - CA, CLK, Ctrl:
    - → Unloaded Section → 45 ohm
    - → Loaded Section → 60 ohm
- Length Matching Method: Velocity Compensation Length Matching

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Routing Geometries

Routing Geometries	RCB (1R x8)
Trace width/spacing (mm) – Unloaded section	
Clock to Clock width/spacing	0.2/0.1
Clock to others spacing	0.3
Control width/spacing	0.2/0.2
CA bus width/spacing	0.2/0.2
Trace width/spacing (mm) - Loaded section	
Clock to Clock width/spacing	0.1/0.1
Clock to others spacing	0.3
Control width/spacing	0.1/0.2
CA bus width/spacing	0.1/0.2
Trace width and spacing – DQ/DM/DQS	
DQ/DM width/spacing	0.1/0.3
DQS/DQS# width/spacing	0.1/0.1
DQS/DQS# to others spacing	0.3

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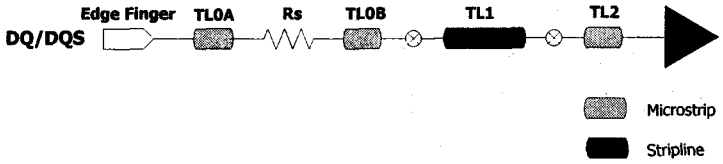
I/O Net Topology



	TL0A		TL0B		TL1		TL2		TOTAL Compensation Length	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
Byte1	3.01	3.42	0.85	3.01	9.91	12.74	0.57	1.47	16.9	16.9
Byte2	3.03	3.58	0.90	2.67	8.33	11.06	0.57	1.47	15.2	15.2
Byte3	2.99	3.69	0.88	2.79	13.12	15.93	0.57	1.47	20.0	20.0
Byte4	2.99	3.24	0.85	2.26	9.50	11.65	0.57	1.47	15.7	15.7
Byte5	2.99	3.32	0.85	2.57	9.13	11.63	0.57	1.47	15.6	15.6
Byte6	2.99	3.47	0.79	2.44	13.00	15.69	0.57	1.47	19.7	19.7
Byte7	3.01	3.39	0.86	2.33	8.52	10.90	0.57	1.47	15.0	15.0
Byte8	3.02	3.23	0.85	2.25	10.61	12.69	0.57	1.47	16.8	16.8

Unit : millimeter

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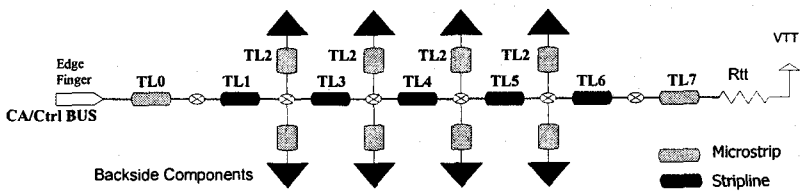
CA/Ctrl Net Topology



CA Bus	TL0	TL1	TL2	TL0+TL1+TL2 Compensation Length	TL3	TL4	TL5	TOTAL Compensation Length TL0+TL1+TL2 TL3+TL4+TL5	TL6	TL7
MIN	29.7	16.54	2.48	76.9	15.2	20.08	15.2	127.4	8.45	0.98
MAX	20.3	72.27	4.96	76.9	15.2	20.08	15.2	127.4	17.89	2.76

CTRL	TL0	TL1	TL2	TL0+TL1+TL2 Compensation Length	TL3	TL4	TL5	TOTAL Compensation Length TL0+TL1+TL2 TL3+TL4+TL5	TL6	TL7
MIN	2.45	71.02	3.55	76.9	15.20	20.80	15.20	127.4	10.33	0.99
MAX	2.58	71.37	4.03	76.9	15.20	20.80	15.20	127.4	15.66	1.16

Unit : millimeter

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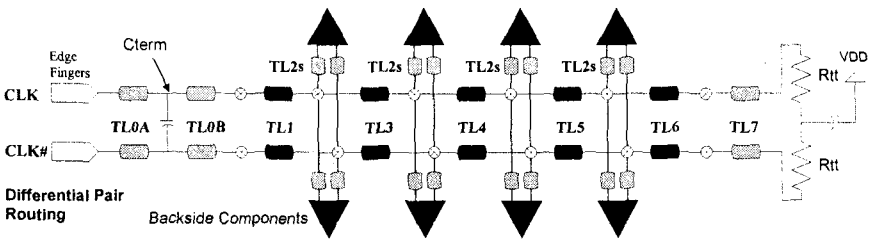
Clock net Topology



	TL0A +TL0B	TL1	TL2	TL0+TL1+TL2 Compensation Length	TL3	TL4	TL5	TOTAL Compensation Length TL0+TL1+TL2 TL3+TL4+TL5	TL6	TL7
MIN	3.94	71.07	2.51	76.9	15.20	20.80	15.20	127.4	14.39	1.12
MAX	3.95	71.07	2.51	76.9	15.20	20.80	15.20	127.4	14.81	1.21

Unit : millimeter

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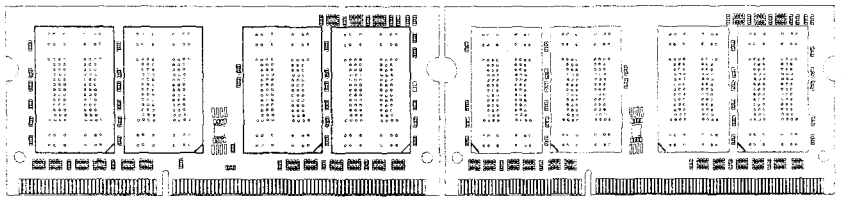
Placement

□ **Front Side**

□ **Back Side**



□ **Passive elements on the module**

Type	Per	Q'ty
VDD-GND Decoupling capacitors	DRAM	4ea
VREF_DQ Decoupling capacitors	DRAM	1ea
VREF_CA Decoupling capacitors	DRAM	1ea
VTT Decoupling capacitors	Two Rtt	1ea
ZQ Resistor	DRAM	1ea

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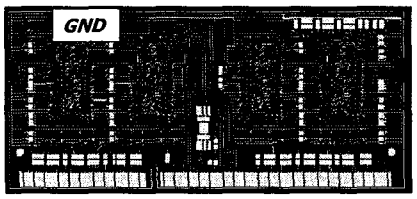
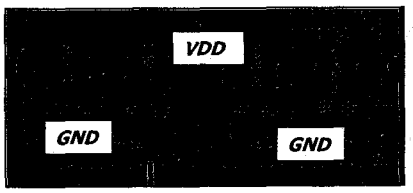
Layer View

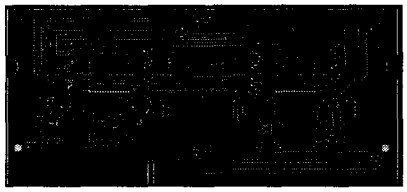
Layer_1



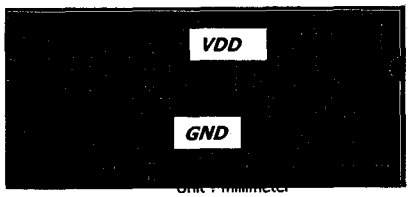
Layer_2



Layer_3



Layer_4



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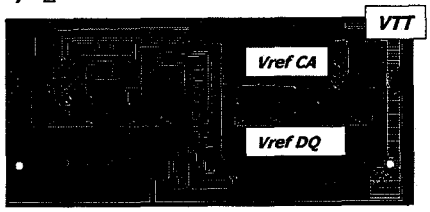
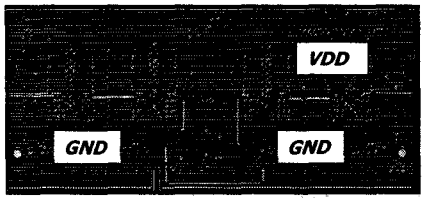
Layer View

Layer_5

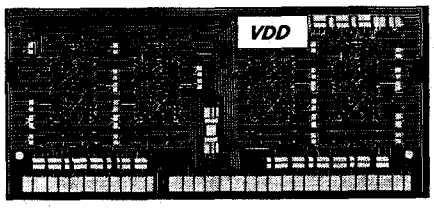
Layer_6



Layer_7



Layer_8



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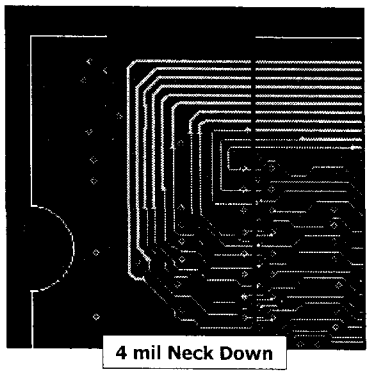
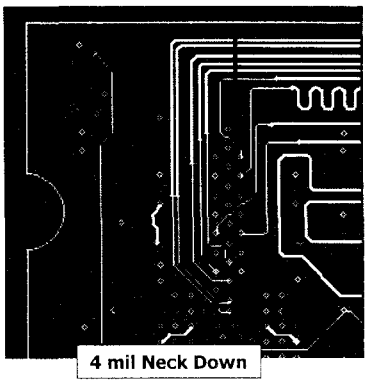
Neck down mode



4 mil Neck Down



4 mil Neck Down

- Neck Down Length Target: 7 mm ~ 8 mm

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APPENDIX
[Verification Simulation]

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Simulation Assumptions

I. Parameter Table

Component	Signal Group	Value		Notes
Frequency	Common	1333MT/s		
VDDQ	Common	1.425V		Slow Corner Case.
MCH	I/O	Ron [Ω]	40	Non-Linear Model – Tolerance : + 40% @0.8 VDDQ
		Clo [pF]	4.5	@1333MHz , [Cdie + Cpkg]
		Drv S/R [V/ns]	2.5~5.0	25Ω, VDD/2 termination
	ADD/CMD/Ctrl	Ron [Ω]	27	Linear Model
		Drv S/R [V/ns]	1.5	25Ω, VDD/2 termination
	CLK	Ron [Ω]	40	Linear Model
		Drv S/R [V/ns]	3.0	
DRAM	I/O	Ron [Ω]	40	Non-Linear Model – Tolerance : + 40% @0.8 VDDQ
		Clo [pF]	2.5	@1333MT/s , [Cdie + Cpkg]
		Drv S/R [V/ns]	2.5~5.0	25Ω, VDD/2 termination
	ADD/CMD/Ctrl	Ci [pF]	1.25	@1333MT/s , [Cdie + Cpkg]
	CLK	Ci [pF]	1.25	@1333MT/s , [Cdie + Cpkg]
MoBo Topology	Common	Length [Inch]	Max 4.5	X-talk : 2500 mil 2W 5-Coupled line. SLOT to SLOT : 0.5"
		Z_{o_MB} [Ω]	40	+/- 15% Tolerance , CLK signal Z_{diff} is 70Ω.
DIMM Topology	Common	Length [Inch]	Based on R/C 'A'	
		Z_{o_MB} [Ω]		
X-talk	Common	5-Coupled[I/O] 3-Coupled[CA/Ctrl]		Input PRBS – Even/odd mode
ODT Tolerance	I/O	60/120Ω	30%	Reff = $(V_{IH(ac)} - V_{IL(ac)})/\lvert I_{IH(ac)} - I_{IL(ac)} \rvert$
		40Ω	50%	

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Simulation Assumptions

II. CLK Signal

1. Differential Impedance Rules
   - → MCH to connector – 60Ω Diff Z_0
   - → Lead-in unloaded section – 60Ω Diff Z_0
   - → Inter-device loaded section – 90Ω Diff Z_0
2. Termination Scheme – Center tap capacitive termination.
   - → Center tap capacitor – 0.1㎌
   - → Two Rtts – 36Ω±10%
   - → Cterm – 2.2pF

III. ADD/CMD/Ctrl Signal

1. 1T timing at 1333 MT/s , 2T timing at 1600MT/s
2. 8mm Neck down[60Ω] at the end of the unloaded section on the DIMM
3. Real channel length based on the R/C 'B' Rev 3.1

IV. Measurement Condition

1. Vac/Vdc level – 175mV/100mV
2. Derated Open Data Window

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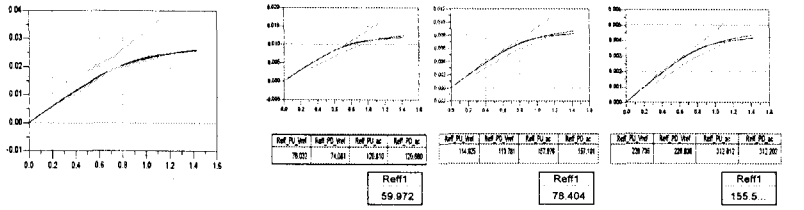
Simulation Models

I. Non-linear Drv & ODT Model for I/O signal group.



[40Ω Drv . - Tolerance Max. 40%] [40Ω - Tolerance Max. 50%]60Ω - Tolerance Max. 30%]120Ω - Tolerance Max. 30%]

1. ODT 40Ω - 50% Tolerance at $[V_{IH}(ac)-V_{IL}(ac)]/|(I_{IH}(ac)-I_{IL}(ac))|$
2. ODT 60Ω/120Ω - 30% Tolerance at $[V_{IH}(ac)-V_{IL}(ac)]/|(I_{IH}(ac)-I_{IL}(ac))|$

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Simulation Result [I/O]

I. I/O Signal

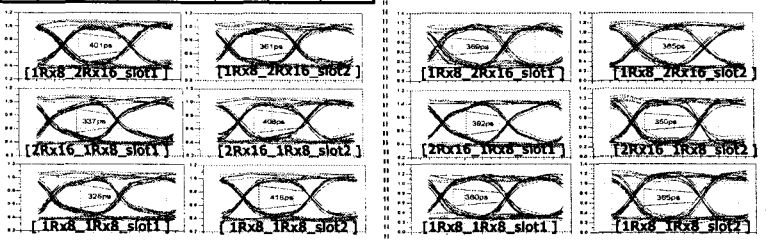
1. ODW values are over **328ps** when using the AC to DC measurement method in the read cases.
2. ODW values are over **350ps** when using the AC to DC measurement method in the write cases.
   → If you look at the timing margin, we think that these values are adequate.

Read ODT Table for Dynamic ODT Scheme

Configuration	Write to..	MCH	Slot1		Slot2	
			1st Rank	2nd Rank	1st Rank	2nd Rank
1R/2R	Slot1	120Ω	Infinite	Unpopulated	40Ω	120Ω
	Slot2	120Ω	40Ω	Unpopulated	Infinite	Infinite
2R/1R	Slot1	120Ω	Infinite	Infinite	40Ω	Unpopulated
	Slot2	120Ω	Infinite	40Ω	Infinite	Unpopulated
1R/1R	Slot1	120Ω	Infinite	Unpopulated	40Ω	Unpopulated
	Slot2	120Ω	40Ω	Unpopulated	Infinite	Unpopulated
1R/NC	Slot1	120Ω	Infinite	Unpopulated	Unpopulated	Unpopulated
NC/1R	Slot1	120Ω	Unpopulated	Unpopulated	Infinite	Unpopulated

Write ODT Table for Dynamic ODT Scheme

Configuration	Write to..	MCH	Slot1		Slot2	
			1st Rank	2nd Rank	1st Rank	2nd Rank
1R/2R	Slot1	Infinite	Infinite	Unpopulated	40Ω	Infinite
	Slot2	Infinite	40Ω	Unpopulated	Infinite	Infinite
2R/1R	Slot1	Infinite	120Ω	Infinite	40Ω	Unpopulated
	Slot2	Infinite	Infinite	40Ω	Infinite	Unpopulated
1R/1R	Slot1	Infinite	Infinite	Unpopulated	40Ω	Unpopulated
	Slot2	Infinite	40Ω	Unpopulated	Infinite	Unpopulated
1R/NC	Slot1	Infinite	60Ω	Unpopulated	Unpopulated	Unpopulated
NC/1R	Slot1	Infinite	Unpopulated	Unpopulated	60Ω	Unpopulated



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Simulation Result [CLK]-1

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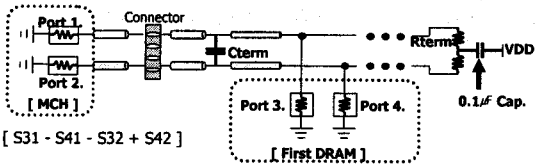
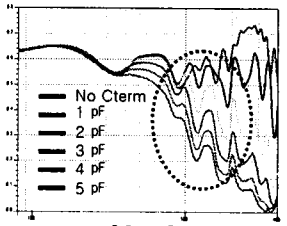
I. FD Analysis

1. S_{DD21}(*Differential to differential*) transfer function analysis at the mixed mode s-parameter.

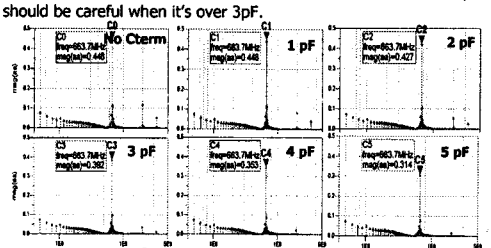


→ S_{DD21} = 0.5 * [S31 - S41 - S32 + S42]

2. As Cterm increases, the signal transfer feature gets worse at the high frequency.
   → Bad transmit feature might be able to bring about the lower slew-rate in time-domain analysis.
   → Looking at the S_{DD21}, we should be careful when it's over 3pF.



[S_{DD21}]



[Time to Frequency Transform]

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Simulation Result [CLK]-2

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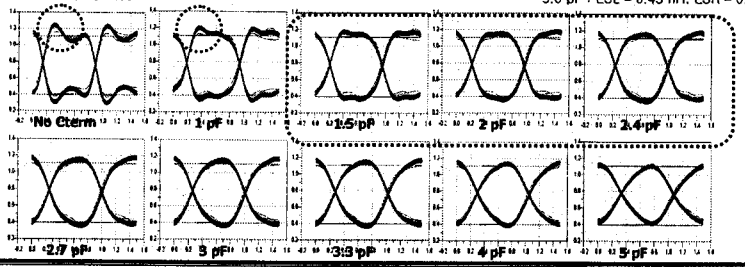
I. Time-domain Analysis

1. Maximum V_{IX} deviation → There are no big differences for V_{IX} deviation between Cterm values.
2. Vref Jitter → As Cterm value increases, the jitter increases.
3. Ledge at the transition point → There are some problems of ledge issues on the transition point with lower Cterm and without Cterm.

DRAM #	1st DRAM									
Cterm [pF]	0.0	1.0	1.5	2.0	2.4	2.7	3.0	3.3	4.0	5.0
Pos. Dev.[mV]	58	58	58	58	58	58	58	57	57	55
Neg. Dev.[mV]	-21	-22	-22	-22	-22	-22	-21	-21	-20	-19
Min. S/R[V/ns]	3.50	2.51	2.32	2.20	2.09	1.99	1.89	1.78	1.54	1.27
Vref Jitter.[ps]	31.5	31.6	35.4	38.2	38.8	41.0	43.2	45.4	51.2	61.1

- Rterm : **Two Rtts 36Ω ±10%**
- Cterm value options [ESL/ESR]
  - 1.0 pF : ESL – 0.49 nH, ESR – 0.181 Ω
  - 1.5 pF : ESL – 0.47 nH, ESR – 0.087 Ω
  - 2.0 pF : ESL – 0.48 nH, ESR – 0.133 Ω
  - 2.4 pF : ESL – 0.48 nH, ESR – 0.126 Ω
  - 2.7 pF : ESL – 0.48 nH, ESR – 0.127 Ω
  - 3.0 pF : ESL – 0.48 nH, ESR – 0.119 Ω
  - 3.3 pF : ESL – 0.48 nH, ESR – 0.114 Ω
  - 4.0 pF : ESL – 0.49 nH, ESR – 0.107 Ω
  - 5.0 pF : ESL – 0.45 nH, ESR – 0.085 Ω

II. Waveform



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Simulation Result [CA Bus]

I. Slew-rate should be limited below 1.5v/ns at least at the low VDD to get a voltage margin without ring back.

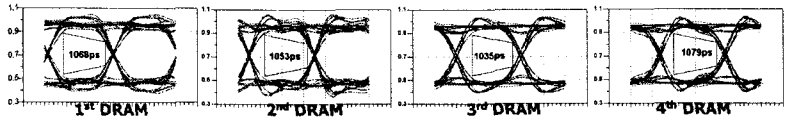
II. 30ohm Rterm is good for the signal integrity compared to 36ohm.

III. Timing Budget Assumptions

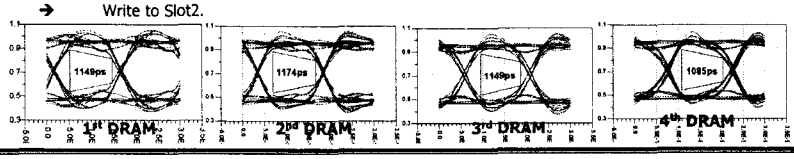
1. ODW > t_{IS} + t_{IH} + CLK Jitter + Timing mismatch between CLK to DRAM.
   - → t_{IS} / t_{IH} : 280ps / 280ps at the Vref level.
   - → Maximum CLK Jitter : 90ps
   - → Timing mismatch between ADD signal and CLK signal: 150ps
   - → **ODW > 800ps at the Vref level**

IV. Eye-diagram

1. ADD/CMD Net in 1Rx8/1Rx8 Configuration [heavy loading case]
   - → Write to Slot1.



   - → Write to Slot2.



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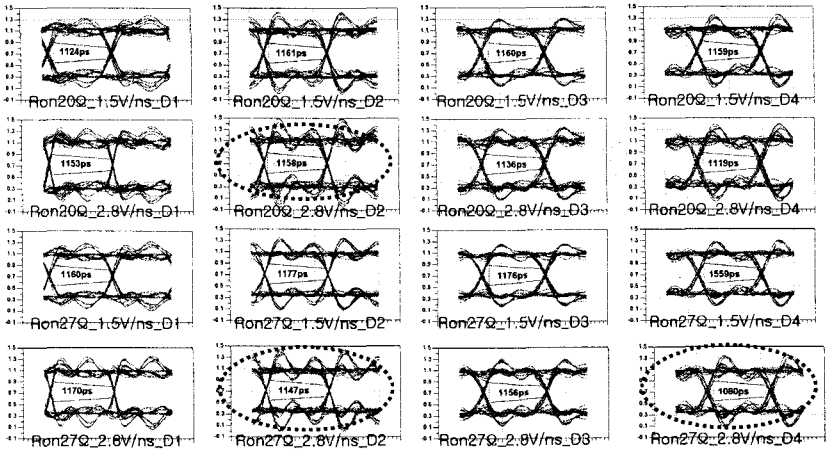
Simulation Result [ctrl]

I. Ring back Issue

1. In order to reduce the ring back, more strong driver and lower slew-rate are needed.



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Summary

- **I/O Signal**
  - We see adequate margin for the RC B design
  - Minimum ODW value is 328ps using AC to DC measurement method for the read case.
  - Minimum ODW value is 350ps using AC to DC measurement method for the write case.
- **CLK Signal**
  - The slew-rate decreases when the Cterm value increases
  - Lower slew-rate could effect delay and jitter.
  - There are some ledge issues during transitions with lower Cterm and without Cterm.
  - Our recommendation for the Cterm value range is between 1.5pF to 2.4pF.
- **ADD/CMD/Ctrl Signal**
  - High output slew-rate at low VDD causes ring back that reduces voltage margin because of x-talk.
  - 30ohm Rterm for the CTRL signal shows a better signal integrity result compared to 36ohm.

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Thank you!!