

**Passive Embedded Substrate for RF
Integrated Package**

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(KETI/Korea)

Passive Embedded Substrate for RF Integrated Package

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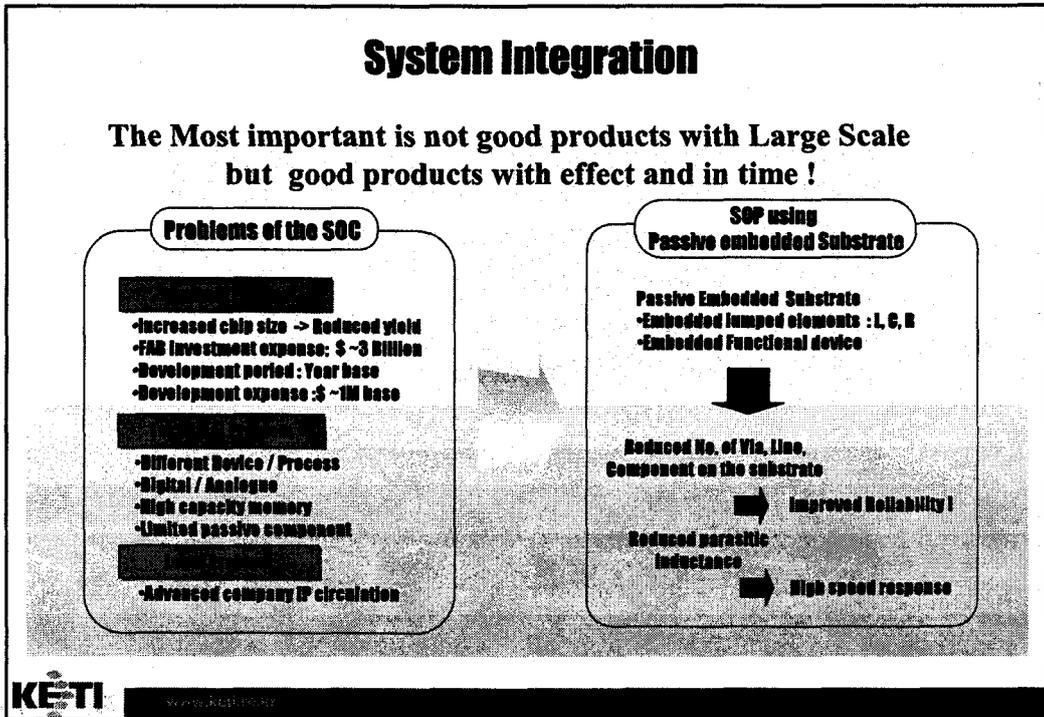
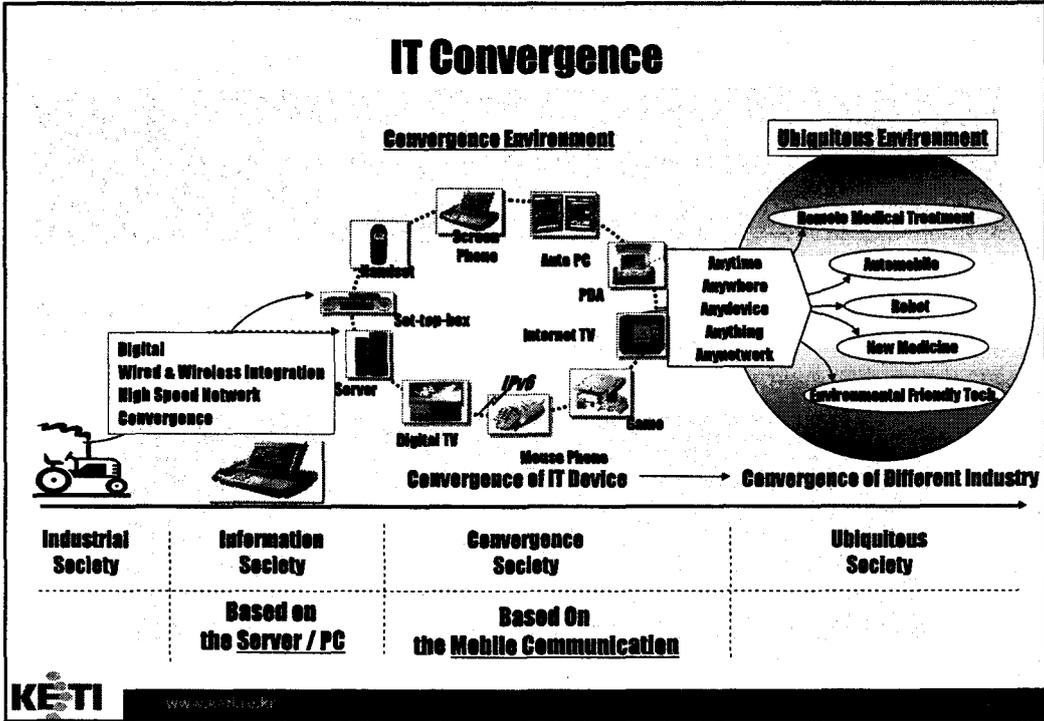
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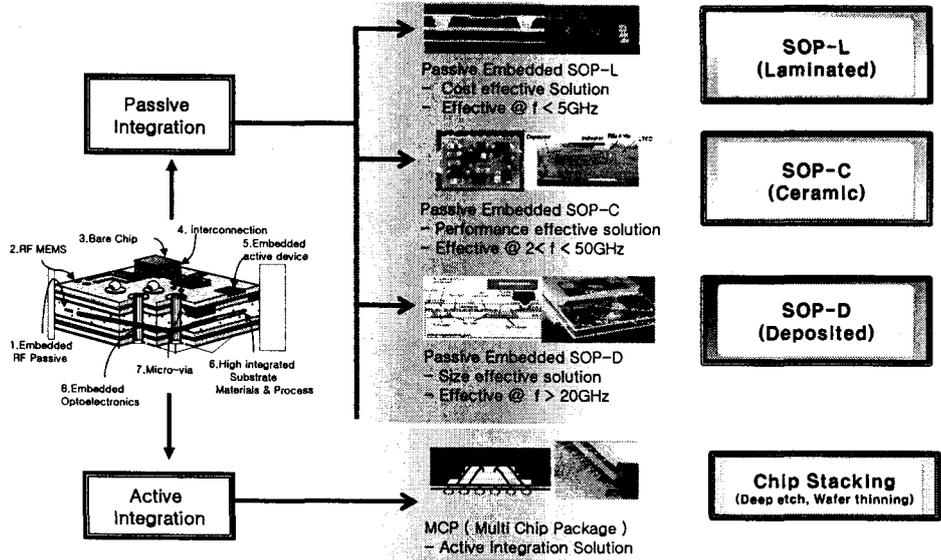
OCT.12. 2006

Outline

- IT Convergence
- System Integration
- CDMA FEM using Passive Embedded Substrates
 - Power Duplexer Module
 - Dual Band Front End Module
- Results

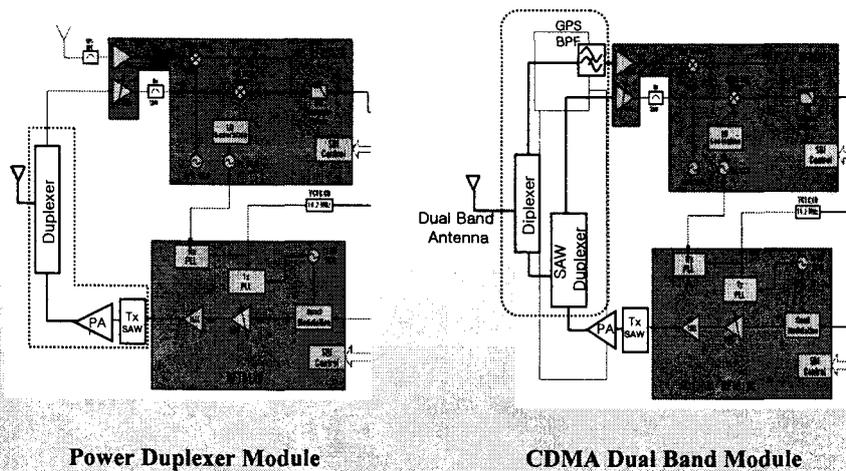


System on Package Process



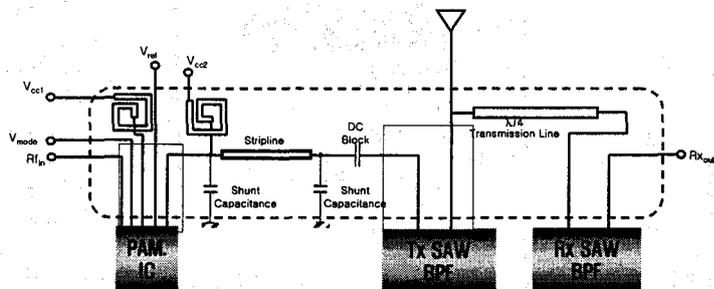
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CDMA FEM using Passive embedded substrate



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Power Duplexer Module



Power Duplexer Module Block Diagram



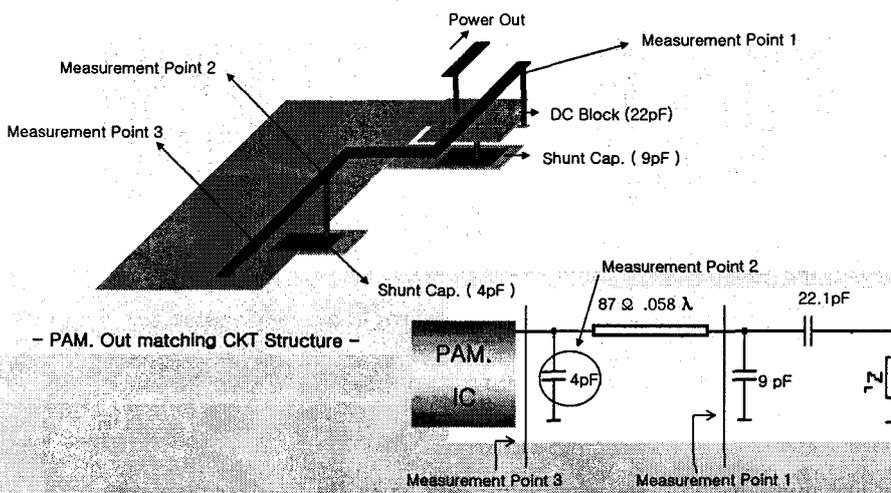
Module 3D Structure

- Embedded Parts
 - 3 Capacitors
 - 2 RF Choke
 - 2 transmission Line
- SMD Parts
 - 2 Bare chip



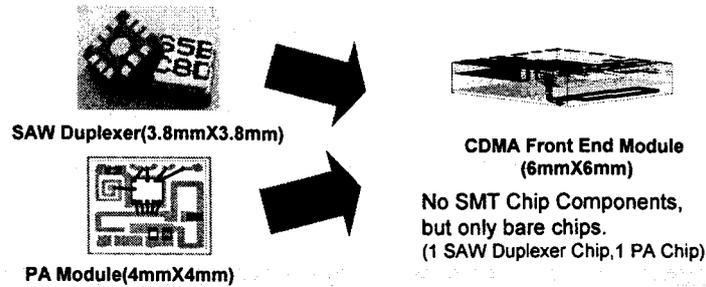
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Measurement Points of the Embedded Parts



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Integration of Duplexer and PA Module



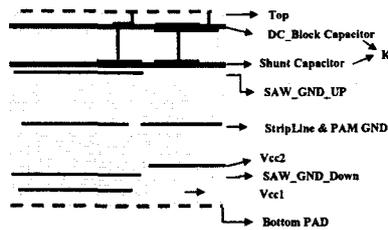
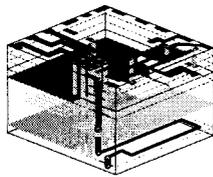
- **High K Material for the Embedding Capacitor**
 - more than double layers or areas are need with $k=7.4$ material
 - Increasing layers or pattern area, decreasing Q value of capacitor
- **Low K Material for the Strip line of the Duplexer**
 - 50Ω line width : $80\mu\text{m}$ with $k=7.4$ material
 - $11\mu\text{m}$ with $K=17.4$ material

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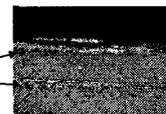
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Fabrication : Co-firing of the Heterogeneous Dielectrics (K17.5/K7.4)

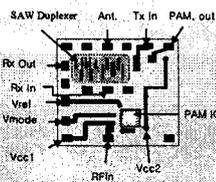
- 3-D structure of Power Duplexer Module : Small Size, High Performance



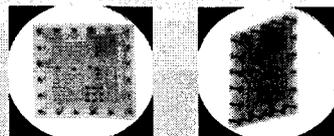
- Embedded Cap. : Paste



Voids after dielectric printing



- X-ray Transparency View



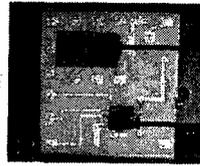
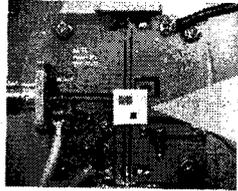
- Embedded Cap. : Green Sheet



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Electrical Characteristics of Power Duplexer Module



SAW Duplexer

Power Amp.

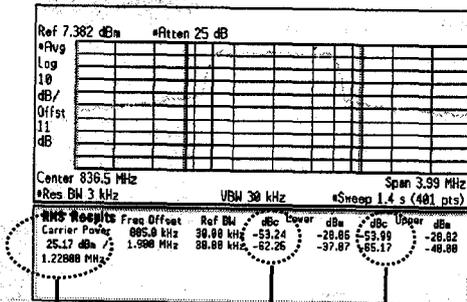
Parameter	Unit	Specification	Note
Output Power Level	dBm	25	Vcc: 3.4V
Gain @25dBm	dB	25.4	
Current / PAE @25dBm	mA	434	Vcc: 3.4V
ACPR1 @885kHz offset	dBc	-52	@25dBm, Vcc: 3.4V
ACPR2 @1.98MHz offset	dBc	-63	@25dBm, Vcc: 3.4V
Idle Current (Quiescent Current)	mA	116	
2 nd Harmonics	dBc	-63	
3 rd Harmonics	dBc	-58	
Tx Isolation	dB	< -47	

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Measurement Plot of Power Duplexer Module

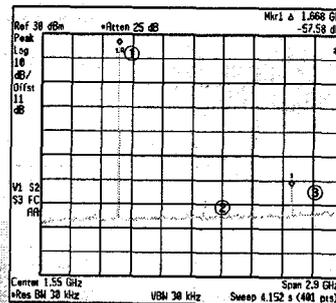
• ACPR Measurement Plot



Carrier Power
@25.17 dBm

ACPR
< -52 dBc @885 kHz
< -62 dBc @1.98 MHz...

• Harmonics Measurement Plot

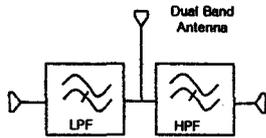


① Fundamental Signal
 ② 2nd Harmonics < -63 dBc
 ③ 3rd Harmonics < -57 dBc

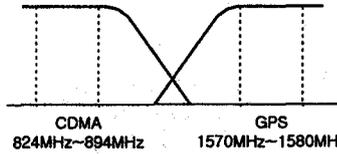
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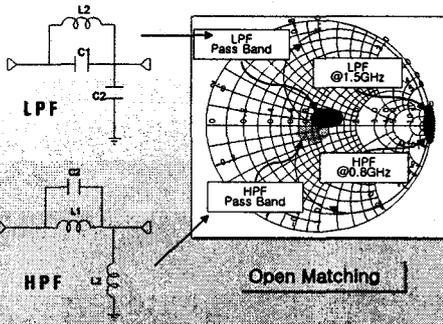
Dual Band module - Diplexer



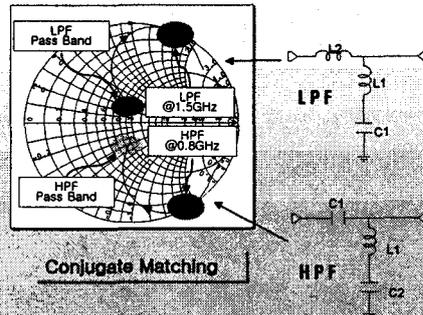
Diplexer



Diplexer Frequency Characteristics



Open Matching

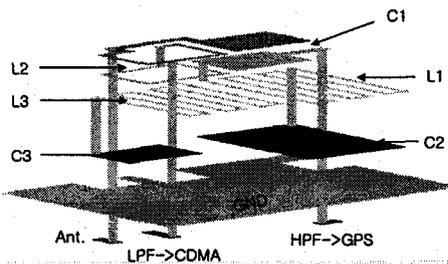
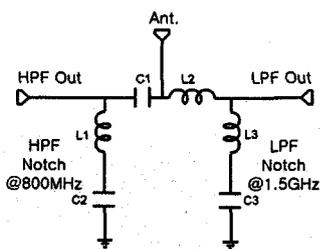


Conjugate Matching

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Dual Band module - Diplexer



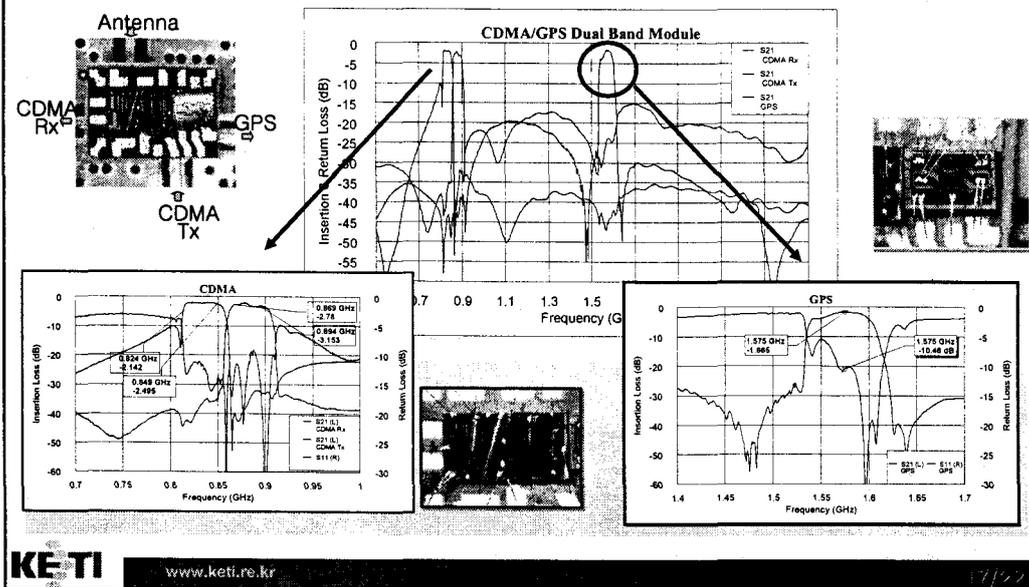
Fabrication

- Pb-Free LTCC ($\epsilon_r=7.5$, $\tan\delta=0.005$, Layer Thickness=35 μm)
- Ag electrode
- Co-Firing Temp. = 860°C
- Insertion Loss = 0.5dB Max (@CDMA Band), 0.6 dB Max. (@GPS Band)

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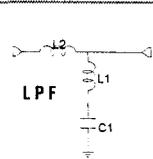
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Dual Band module (With CDMA Duplexer & GPS SAW Filter)

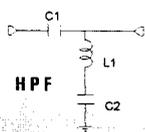


Design & Simulation of the Embedded Passives

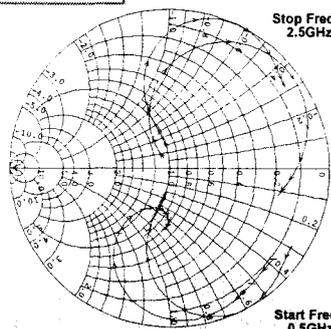
Design with ideal L,C elements



Schematic of LPF
(With ideal L,C)

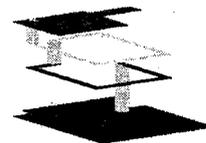
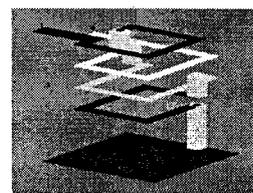


Schematic of HPF
(With ideal L,C)



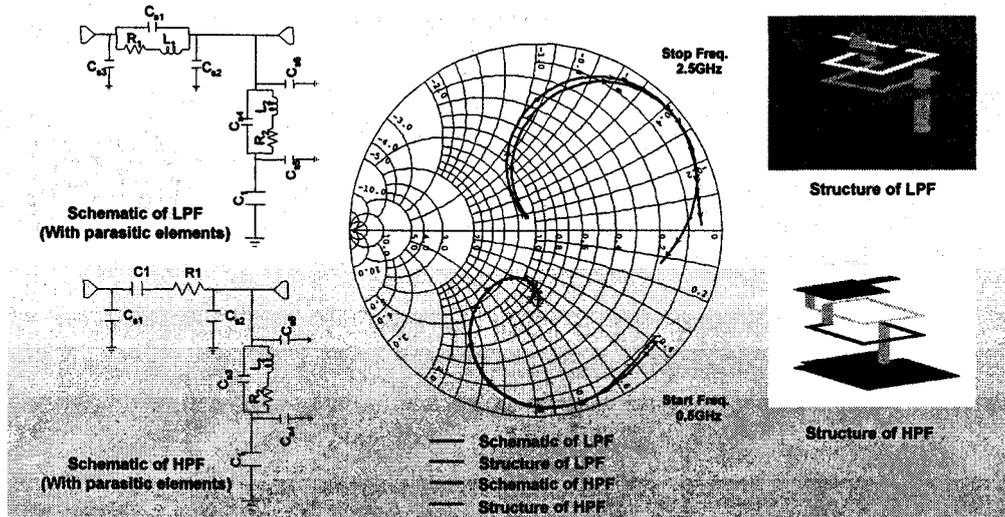
- Schematic of LPF
- Structure of LPF
- Schematic of HPF
- Structure of HPF

Difference between
schematics & structures



Design & Simulation of the Embedded Passives

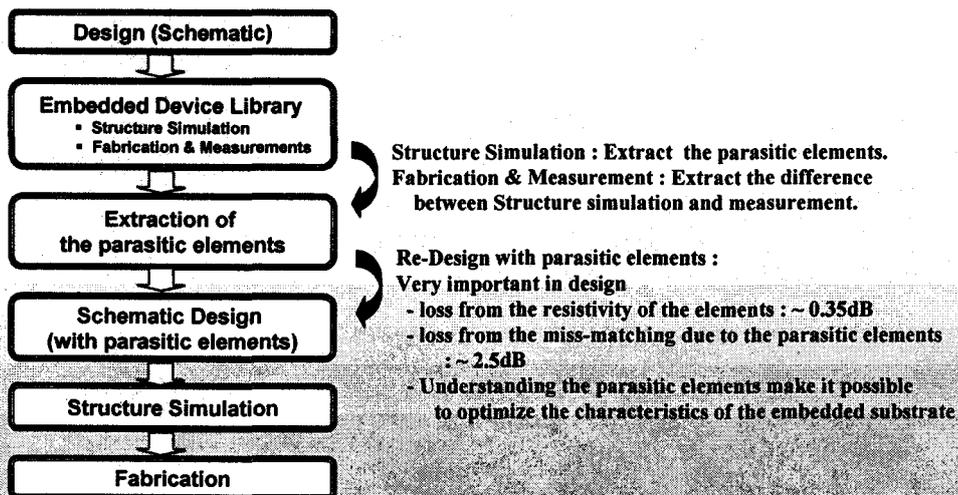
Design with elements including parasitic effects



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Design & Fabrication Flow of the Passive Embedded Substrate



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Conclusions

- **Many possibilities to realize better performance.**
 - Using conjugate matching, less efforts needed to optimize the characteristic of the individual components.
 - In the case of Power Duplexer module, advantages in harmonic characteristics of the amplified signal and ACPR characteristics.
 - In the case of CDMA/GPS dual Band Module, total insertion loss is less than the summation of the losses of the individual filters.
- **Duplexers & Filters with SAW& BAW is essential(commercial mobile communication.)**
- **Filters with LTCC is the effective solution (Freq. Range > 2GHz)**
- **High integration is possible using co-firing heterogeneous dielectrics.**
- **More efforts needed to understanding parasitic effects.**



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Thank you!



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