Toward the 3D-SiP Era with New Technologies

Morihiro Kada

(Sharp/Japan)

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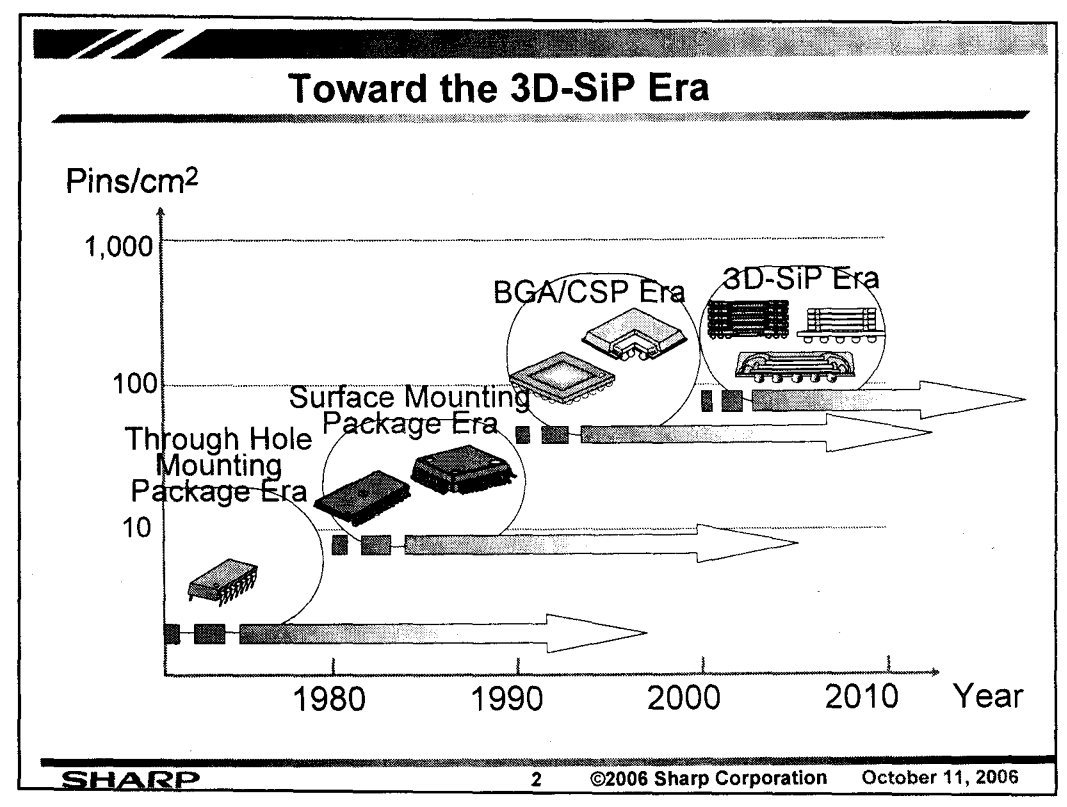
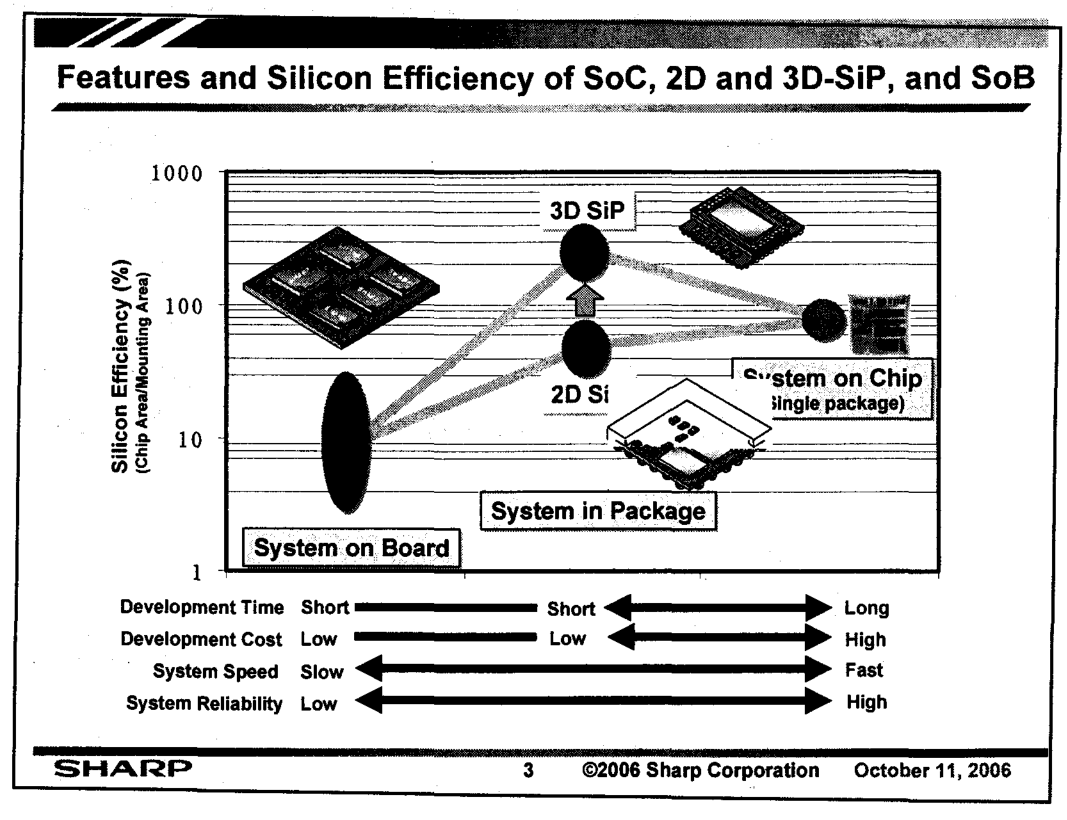
Morihiro Kada
Assembly and Packaging Development Dept.
Sharp Corporation

Toward the 3D-SiP Era




Features and Silicon Efficiency of SoC, 2D and 3D-SiP, and SoB
1000
100
10
1
Silicon Efficiency (%)
(Chip Area/Mounting Area)
3D SiP
2D Si
System on Chip
(Single package)
System in Package
System on Board
Development Time Short Short Long
Development Cost Low Low High
System Speed Slow Fast
System Reliability Low High
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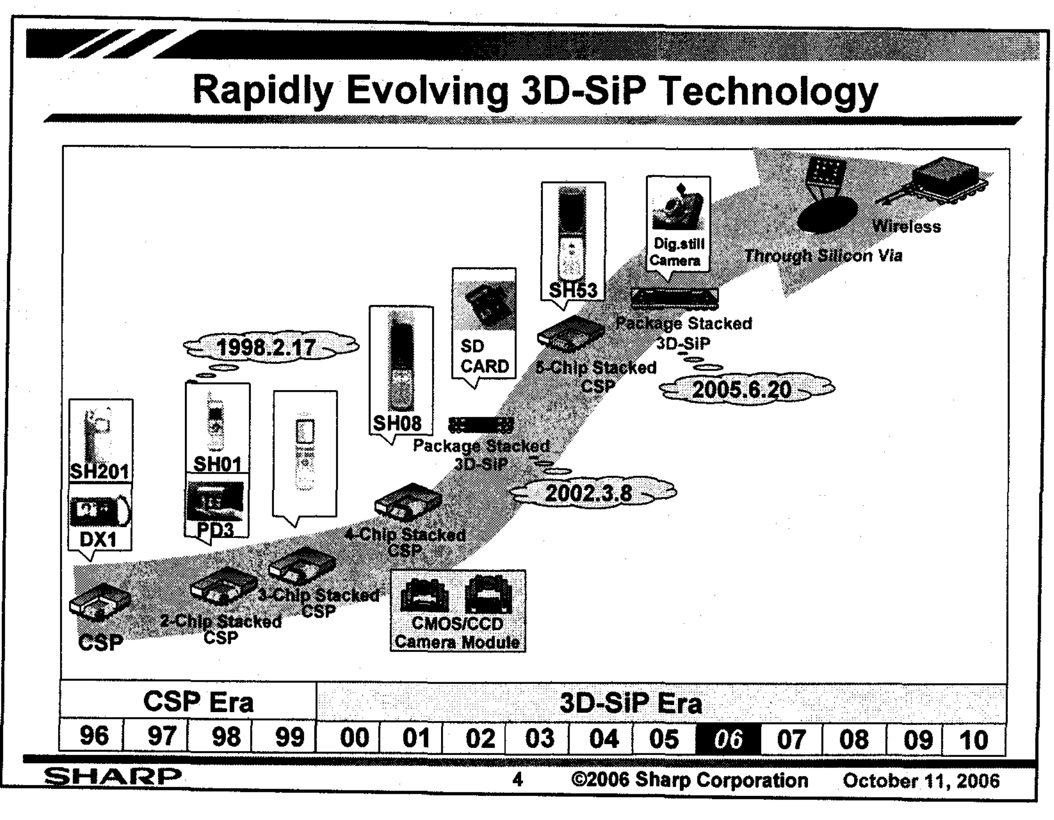
Rapidly Evolving 3D-SiP Technology
Wireless
Through Silicon Via
Dig.still Camera
SH53
Package Stacked 3D-SiP
SD CARD
8-Chip Stacked CSP
2005.6.20
1998.2.17
SH08
Package Stacked 3D-SiP
2002.3.8
SH201
SH01
DX1
PD3
4-Chip Stacked CSP
3-Chip Stacked CSP
2-Chip Stacked CSP
CSP
CMOS/CCD Camera Module
CSP Era
3D-SiP Era
96 97 98 99 00 01 02 03 04 05 06 07 08 09 10
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Chip stack and Package stack

Stacked Die vs. PoP – Trade Offs

Stacked Die	PoP
Prospects • IDM ownership • Smaller body size and lower package profile	***Prospects*** • OEM Ownership • Flexible memory sources, facilitate memory capacity increases • **Tested at individual package level for Known Good Device**
Concerns • KGD required for high product yield • Single-sourced product • New development needed to change a device or handle die shrink • Compound yield and multi test	*Concerns* • Slightly larger / thicker Package stack • Co-design for bottom and top packages • Infrastructure for package stacking

Source: Amkor Technology, Panasonic Factory Solutions, Senju Metal Industry, Sharp (ECTC2006)

Chip Stacking Technology

Pyramid Stacking Structure

Normal Wire Bonding (Left) and Reverse Wire Bonding (Right)

Over Hanging Stacking Structure

Chip on Wire (Cow) technology

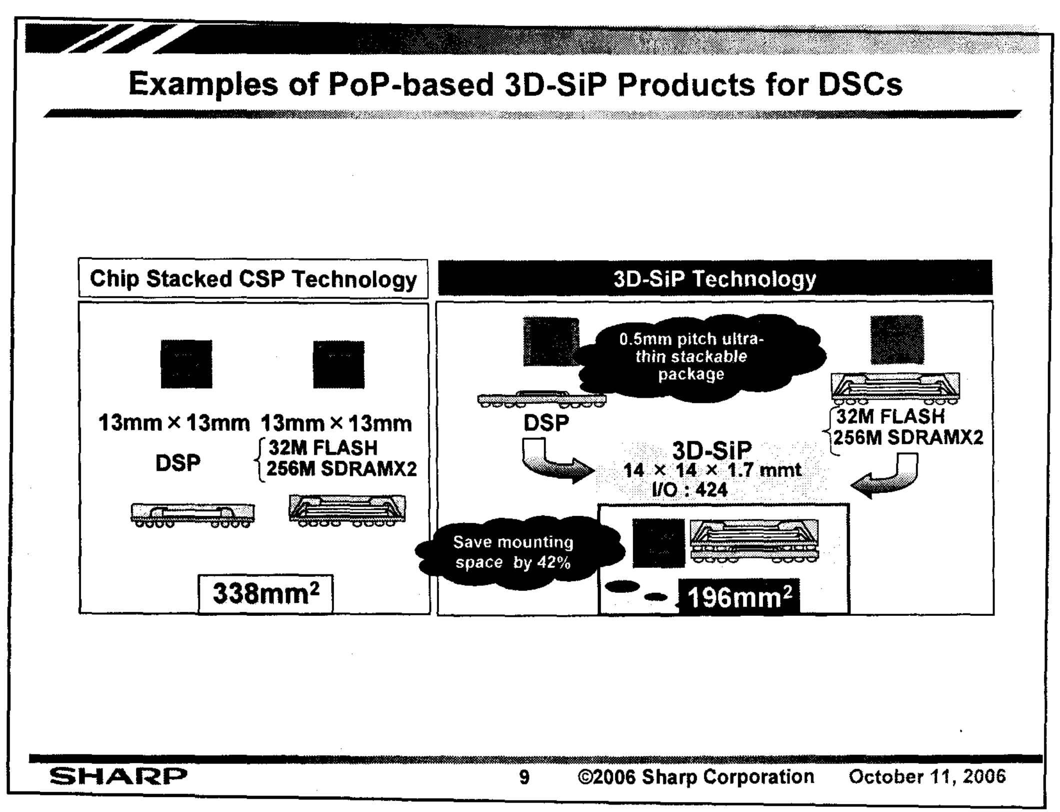
Overview of Package-Stacking Technologies (Logic + Memory)

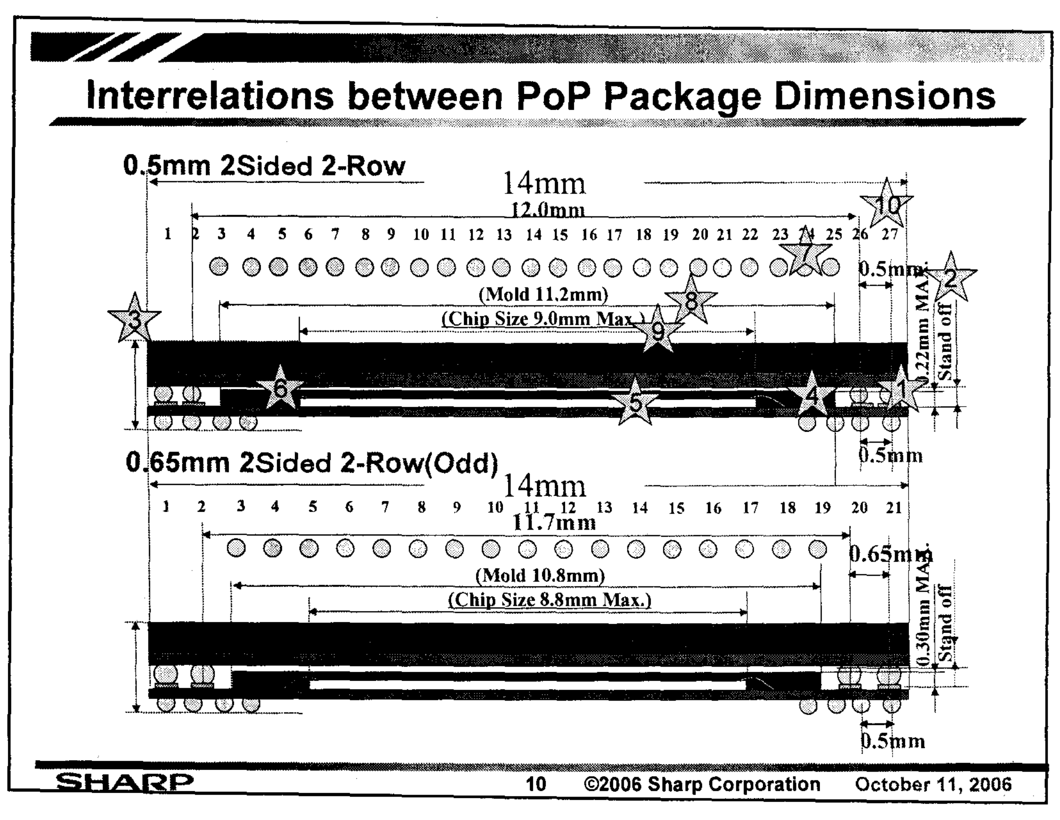
	Fan-out+Solder Ball Interconnect (Sharp etc)	Tape Substrate Interconnect (A)	ISM+ Wire Bond Interconnect (B)
Ownership	Customer	Logic Manufacture	Logic Manufacture
Ex. Package Top Memory Bottom Logic	14X14 0.5P(2S/3R) 162max 0.5P(4S/2R) 200max 0.5P 436max (0.65P) (385max)	13X11 0.65P 188 14X14 0.65P 336	14X14 13X13
Package Height (1Logic+2memory)	1.60max	1.55max	
Production Line	Conventional +	Conventional ++	Conventional ++
Die Shrink	O	O	O
Memory Testing	Δ New Socket	O Current Testing System	× New C/K, New Socket
Multi-layer Stacking	O	Δ	X
Thermal performance	Δ	Δ	Δ
Total Assessment	O	Δ	×

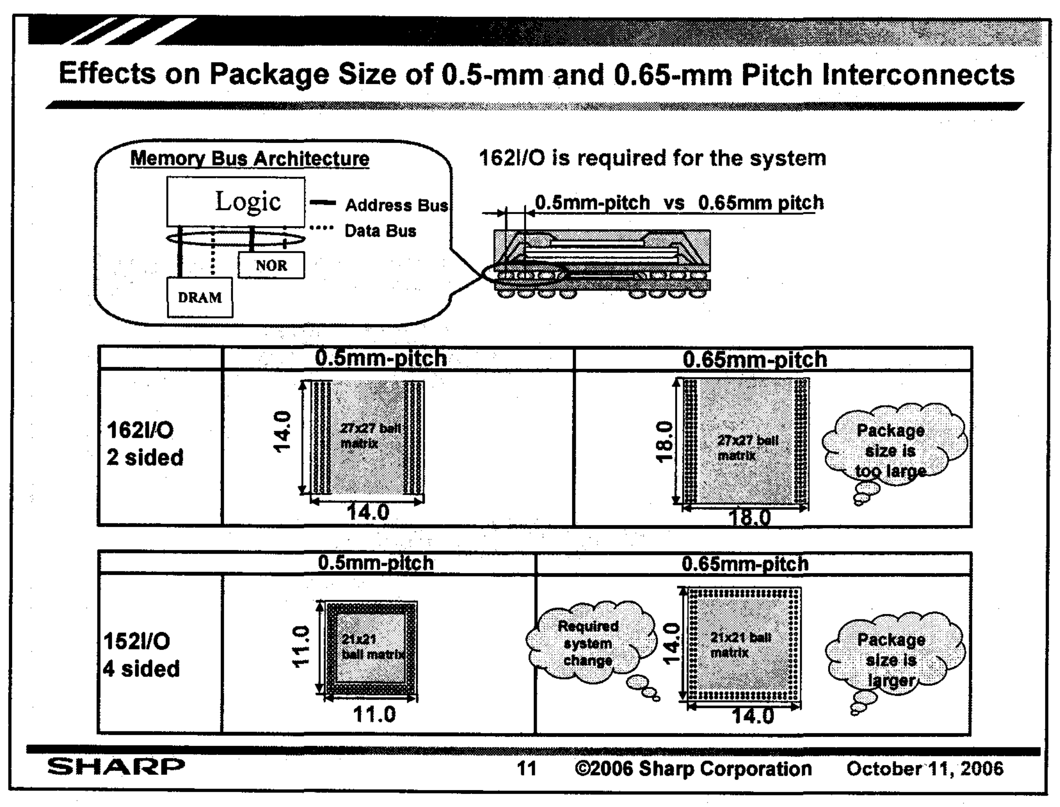
O Good
Δ Fair
X Poor

Features of PoP and PiP

PoP	PiP
1. Uses solder ball (SMT infrastructure) to interconnect individual package. 2. Products are controlled by the customer. 3. Diverse combinations are available without additional infrastructure. 4. Packages are usually larger in size.	1. Uses wire bonding to interconnect individual package. 2. Products are controlled by the Logic manufacture. 3. Diverse combinations are available with additional ISM. 4. Packages are usually smaller in size.


Examples of PoP-based 3D-SiP Products for DSCs
Chip Stacked CSP Technology
13mm×13mm 13mm×13mm
DSP
32M FLASH
256M SDRAMX2
338mm²
3D-SiP Technology
0.5mm pitch ultra-thin stackable package
DSP
32M FLASH
256M SDRAMX2
3D-SiP
14 × 14 × 1.7 mmt
I/O : 424
Save mounting space by 42%
196mm²


Interrelations between PoP Package Dimensions
0.5mm 2Sided 2-Row
14mm
12.0mm
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
0.5mm
(Mold 11.2mm)
(Chip Size 9.0mm Max.)
0.22mm MAX.
Stand off
0.5mm
0.65mm 2Sided 2-Row(Odd)
14mm
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
11.7mm
0.65mm
(Mold 10.8mm)
(Chip Size 8.8mm Max.)
0.30mm MAX.
Stand off
0.5mm


Effects on Package Size of 0.5-mm and 0.65-mm Pitch Interconnects
Memory Bus Architecture
Logic
Address Bus
Data Bus
NOR
DRAM
162I/O is required for the system
0.5mm-pitch vs 0.65mm pitch
0.5mm-pitch
0.65mm-pitch
162I/O
2 sided
14.0
27x27 ball matrix
18.0
Package size is too large
152I/O
4 sided
11.0
21x21 ball matrix
Required system change
Package size is larger
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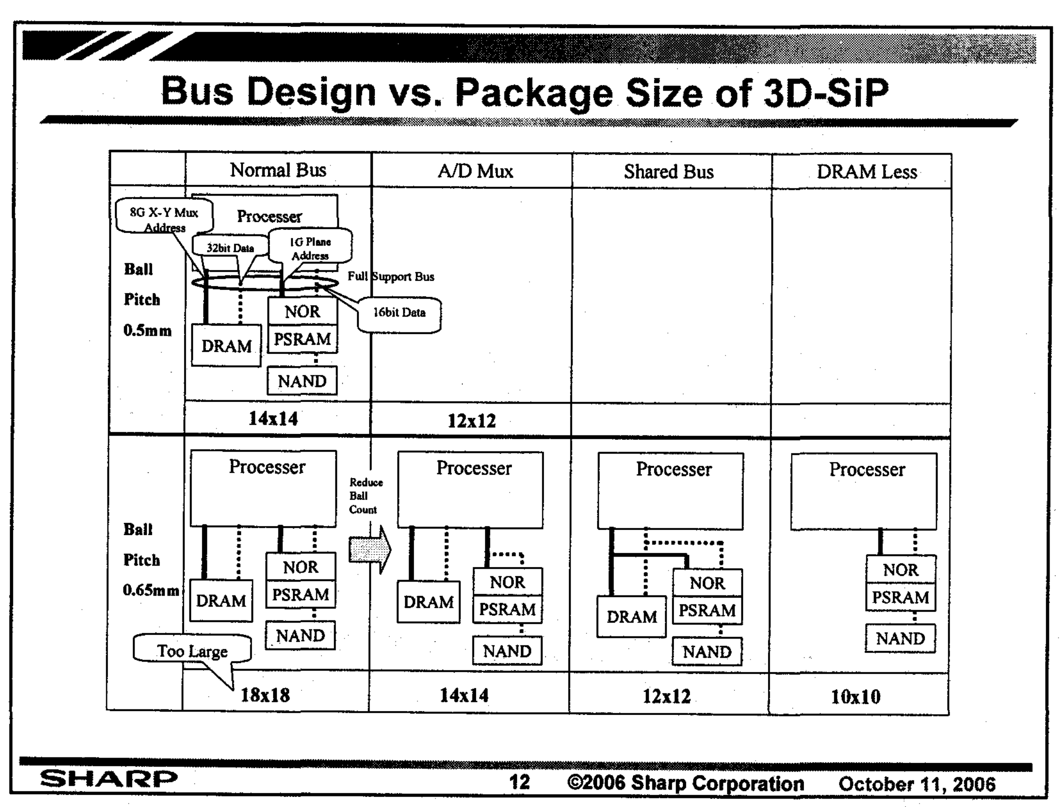
Bus Design vs. Package Size of 3D-SiP
Normal Bus
A/D Mux
Shared Bus
DRAM Less
8G X-Y Mux Address
Processer
32bit Data
1G Plane Address
Full Support Bus
16bit Data
Ball Pitch 0.5mm
NOR
DRAM
PSRAM
NAND
14x14
12x12
Ball Pitch 0.65mm
Reduce Ball Count
Too Large
18x18
14x14
12x12
10x10
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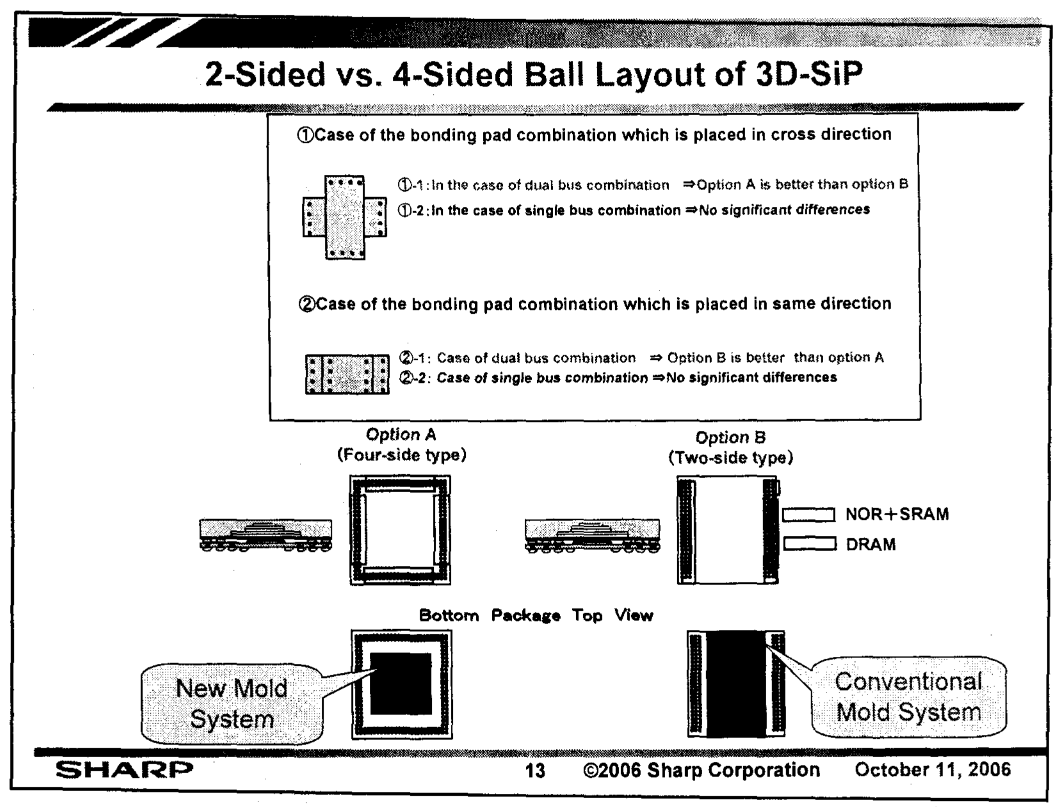
2-Sided vs. 4-Sided Ball Layout of 3D-SiP
①Case of the bonding pad combination which is placed in cross direction
①-1 : In the case of dual bus combination ⇒Option A is better than option B
①-2 : In the case of single bus combination ⇒No significant differences
②Case of the bonding pad combination which is placed in same direction
②-1 : Case of dual bus combination ⇒ Option B is better than option A
②-2 : Case of single bus combination ⇒No significant differences
Option A
(Four-side type)
Option B
(Two-side type)
NOR+SRAM
DRAM
Bottom Package Top View
New Mold System
Conventional Mold System
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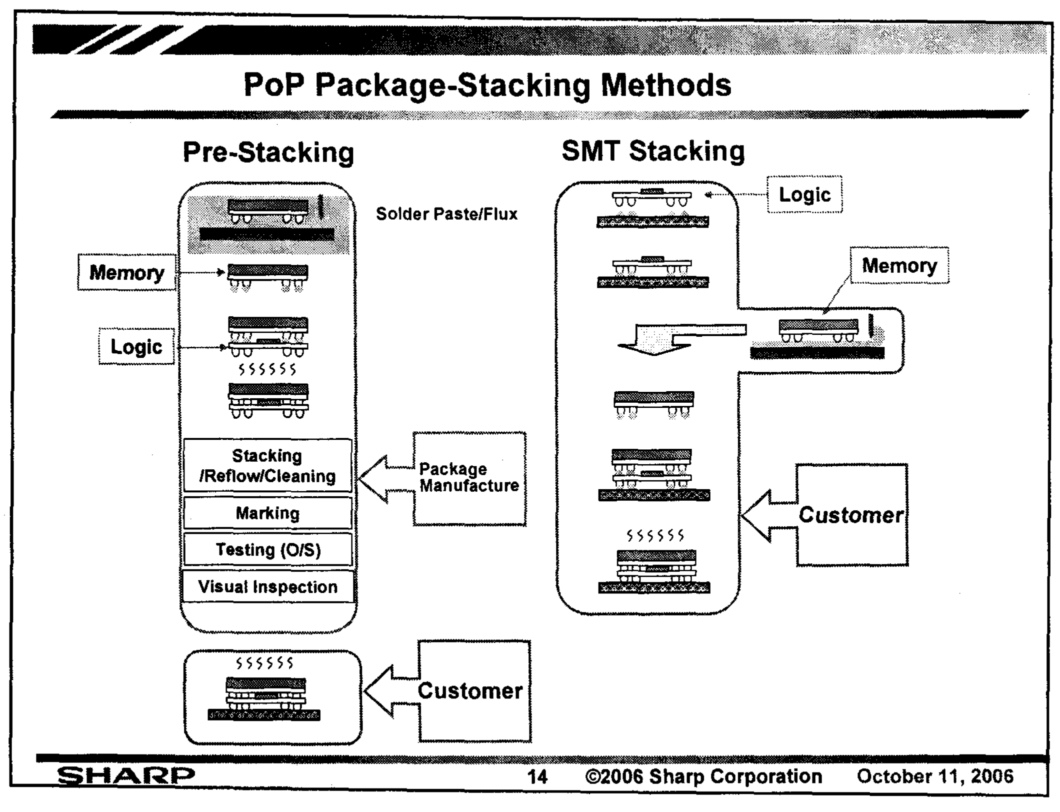
PoP Package-Stacking Methods
Pre-Stacking
SMT Stacking
Solder Paste/Flux
Memory
Logic
Stacking /Reflow/Cleaning
Marking
Testing (O/S)
Visual Inspection
Package Manufacture
Customer
Logic
Memory
Customer
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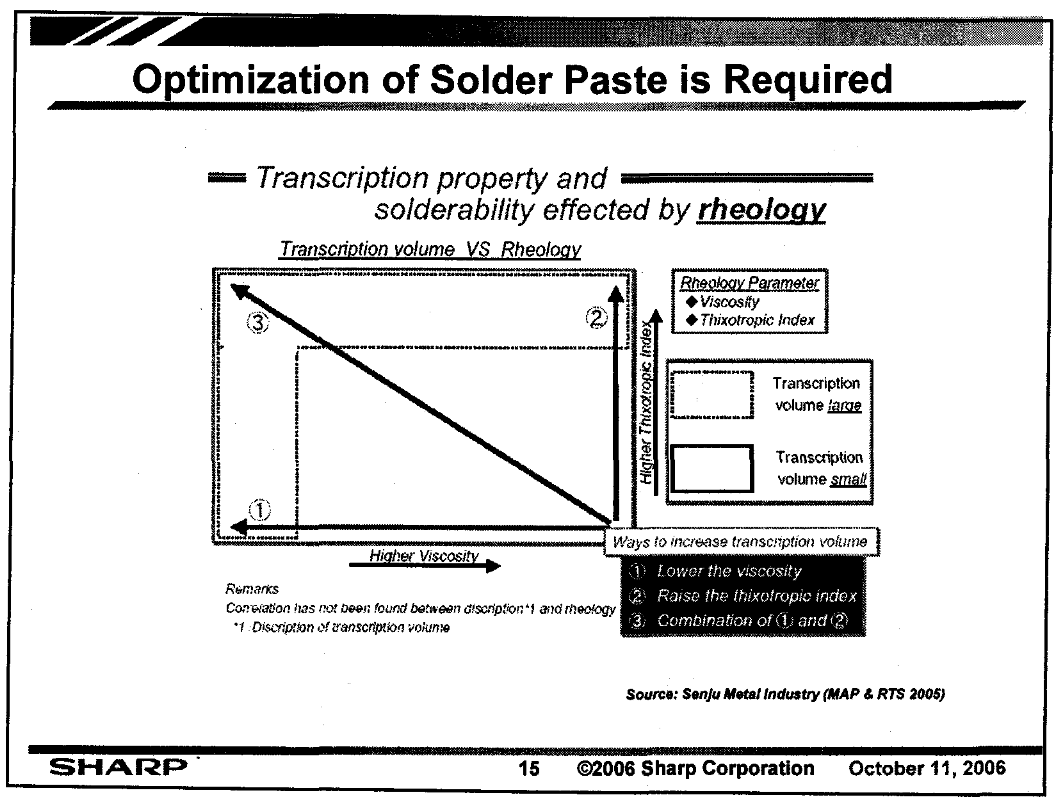
Optimization of Solder Paste is Required
Transcription property and
solderability effected by rheology
Transcription volume VS Rheology
Rheology Parameter
◆Viscosity
◆Thixotropic Index
Transcription volume large
Transcription volume small
Higher Thixotropic Index
Higher Viscosity
Ways to increase transcription volume
① Lower the viscosity
② Raise the thixotropic index
③ Combination of ① and ②
Source: Senju Metal Industry (MAP & RTS 2005)
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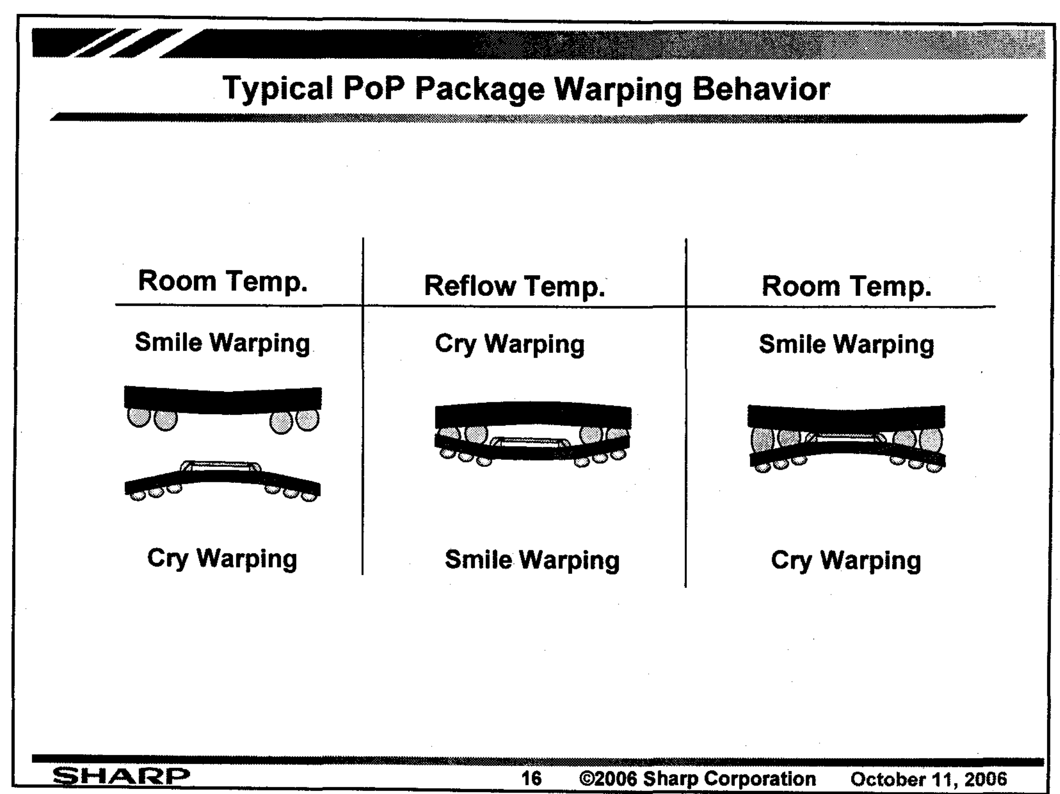
Typical PoP Package Warping Behavior
Room Temp.
Smile Warping
Cry Warping
Reflow Temp.
Cry Warping
Smile Warping
Room Temp.
Smile Warping
Cry Warping
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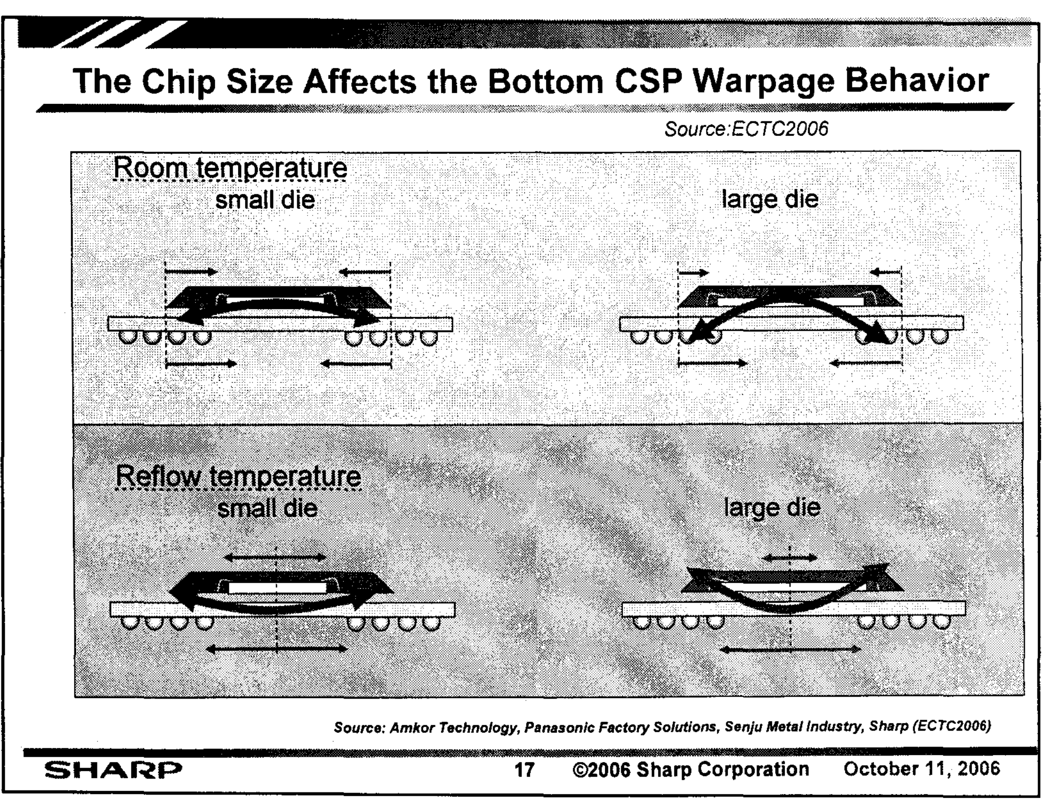
The Chip Size Affects the Bottom CSP Warpage Behavior
Source:ECTC2006
Room temperature
small die
large die
Reflow temperature
small die
large die
Source: Amkor Technology, Panasonic Factory Solutions, Senju Metal Industry, Sharp (ECTC2006)
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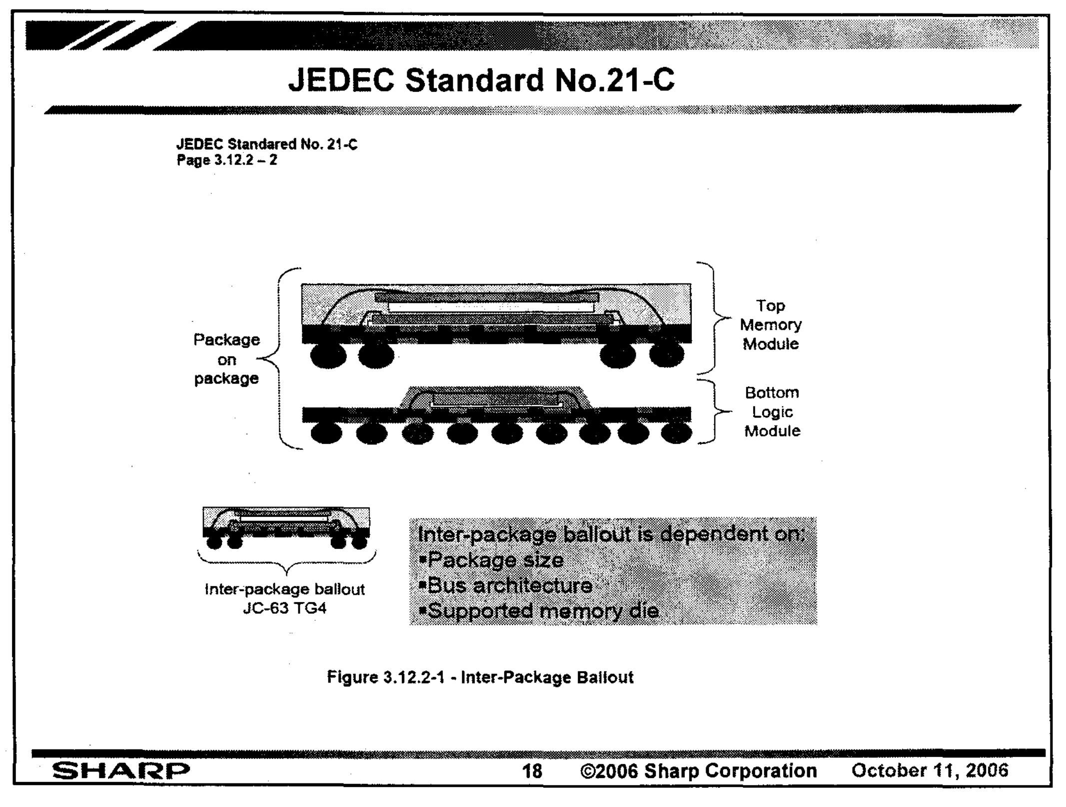
JEDEC Standard No.21-C
JEDEC Standared No. 21-C
Page 3.12.2 – 2
Package on package
Top Memory Module
Bottom Logic Module
Inter-package ballout
JC-63 TG4
Inter-package ballout is dependent on:
▪Package size
▪Bus architecture
▪Supported memory die
Figure 3.12.2-1 - Inter-Package Ballout
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Summary of Standardization of PoP Memory from JEDEC JC-63

JEDEC Standard No.21-C

	Package	Memory Bus Supported
1	11 mm x11 mm Package 0.65 mm Ball Pitch 2 Perimeters of Balls - 112 Total Balls	x16 Nor +x16(p)SRAM +x16 SDRAM +x16 NAND shared databus
2	12 mm x12 mm Package 0.65 mm Ball Pitch 2 Perimeters of Balls - 128 Total Balls	x16 Nor +x16(p)SRAM + x16 SDRAM + x16 NANDshared databus
3	15.00 mm x15 mm Package 0.65 mm Ball Pitch 2 Perimeters of Balls - 160 Total Balls	Options / Bus A / Bus B A: x16 NOR+PS+NAND / x16 DDR B: x16A/D NOR+PS+NAND / x16 DDR C: x32A/D NOR+PS+NAND / x16 DDR D: x16A/D NOR+PS+NAND / x32 DDR
4	16.00 mm x16 mm Package 0.65 mm Ball Pitch 2 Perimeters of Balls - 176 Total Balls	Options / Bus A / Bus B A: x16 NOR+PS+NAND / x16 DDR B: x16A/D NOR+PS+NAND / x16 DDR C: x32A/D NOR+PS+NAND / x16 DDR D: x16A/D NOR+PS+NAND / x32 DDR
5	14 mm x14 mm Package 0.5 mm Ball Pitch 2 Perimeters of Balls - 200 Total Balls	x16 Nor +x16(p)SRAM and x32 SDRAM Split Data Bus
6	14mm x14mm Package 0.65mm Ball Pitch 21 x21 Ball Matrix 152 FBGA	Options / Bus A / Bus B / Bus C AA: x32 (Lower 16 bits) M-DRAM + NOR / x32 (Upper 16 bits) M-DRAM + NOR / x16 NAND AB: x32 (Lower 16 bits) NOR +pSRAM / x32 (Upper 16 bits) NOR + pSRAM / x16 NAND AC: x16 M-DRAM / x16 ADQ NOR / x16NAND AD: None / x16 ADQ NOR +pSRAM / x16NAND
7	13mm x13mm Package 0.65mm Ball Pitch 19 x19 Ball Matrix 136 FBGA	Options / Bus A / Bus B / Bus C AA: x32 (Lower 16 bits) M-DRAM + NOR / x32 (Upper 16 bits) M-DRAM + NOR / x16 NAND AB: x32 (Lower 16 bits) NOR +pSRAM / x32 (Upper 16 bits) NOR + pSRAM / x16 NAND AC: x16 M-DRAM / x16 ADQ NOR(A24 Max) / x16NAND AD: None / x16 ADQ NOR +pSRAM / x16NAND

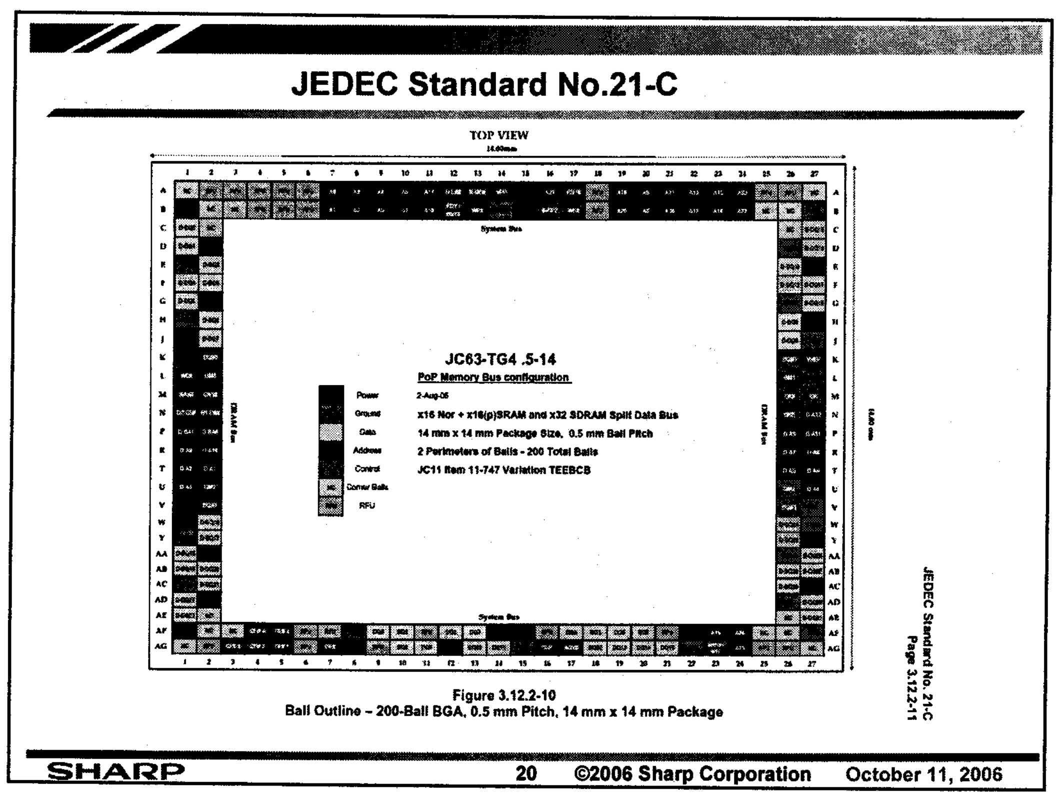

Figure 3.12.2-10
Ball Outline - 200-Ball BGA, 0.5 mm Pitch, 14 mm x 14 mm Package

JEDEC PUBLICATIONS 95 Design Guide 4.22

JEDEC DESIGN STANDARD

DESIGN REQUIREMENTS FOR OUTLINES OF
SOLID STATE AND RELATED PRODUCTS

JEDEC PUBLICATION 95

Design Guide 4.22

Fine-pitch, Square Ball Grid Array Package
(FBGA) Package-on-Package (PoP)

JEDEC
SOLID STATE TECHNOLOGY ASSOCIATION

Date: November 2005 Issue: A
Item: 11.02-726S

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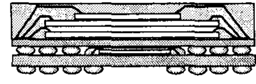
Current and Future Issues in PoP

- Full-fledged use of PoP only have just begun, many issues still remain, such as
  - -Device supply
  - -Expansion of standardization
  - -Stacking infrastructure improvement
- There are also fundamental issues:
  - -Current PoP packages are stacked with a fan-out structure, package size is larger than in chip stacking,
  - -The top package is often memory, for which a chip stack package is used, while a single chip is used for the bottom package to keep package height low.



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New Stack Interconnect Technology

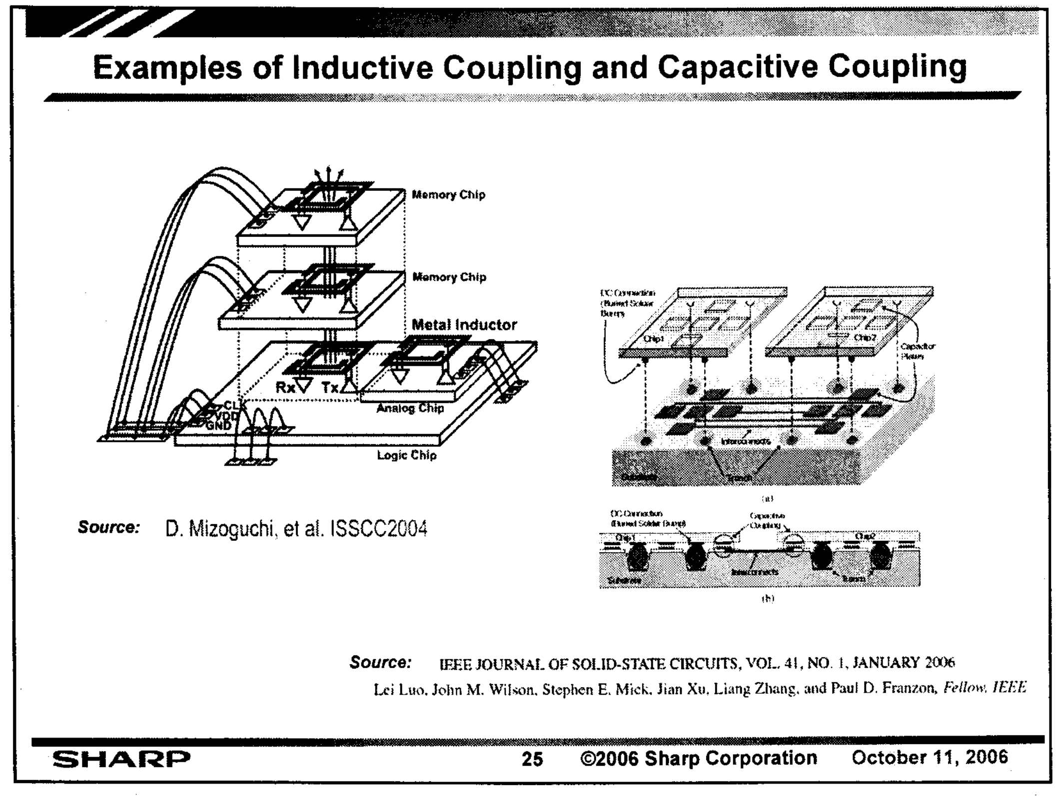
Chip and package stacking have already been adopted commercially and are core technologies in 3D-SiP,but new technologies are starting to gain attention. These can be divided into the following three categories:

1. Through-Silicon Via Technology
   - Chip on Chip
   - Chip on Wafer
   - Wafer on Wafer
2. Wireless Interconnect Technology
   - Inductive Coupling
   - Capacitive Coupling
   - Electromagnetic Wave Coupling
3. Optical Interconnect Technology

Categories of New Interconnect Technologies

	Monolithic	Interchip	Board Level Interconnect
Wired Interconnect	Multilayer Metal Transmission Line	Bonding Wire Through Si Via	PCB Transmission Line Cable: coaxial cable, Flat
Wireless Interconnect		Inductive (L) Coupling Short Distance Capacitive (C) Coupling Very Short Distance	
	Electromagnetic Coupling (Antenna) Long Distance		
Optical Interconnect	Integrated Optical Device Planar waveguide	Optical Circuit Board	Optical Fiber

Source: Iwata (Hiroshima Univ.)


Examples of Inductive Coupling and Capacitive Coupling
Memory Chip
Memory Chip
Metal Inductor
Rx Tx
Analog Chip
Logic Chip
CLK
VDD
GND
Source: D. Mizoguchi, et al. ISSCC2004
Source: IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 1, JANUARY 2006
Lei Luo, John M. Wilson, Stephen E. Mick, Jian Xu, Liang Zhang, and Paul D. Franzon, Fellow, IEEE
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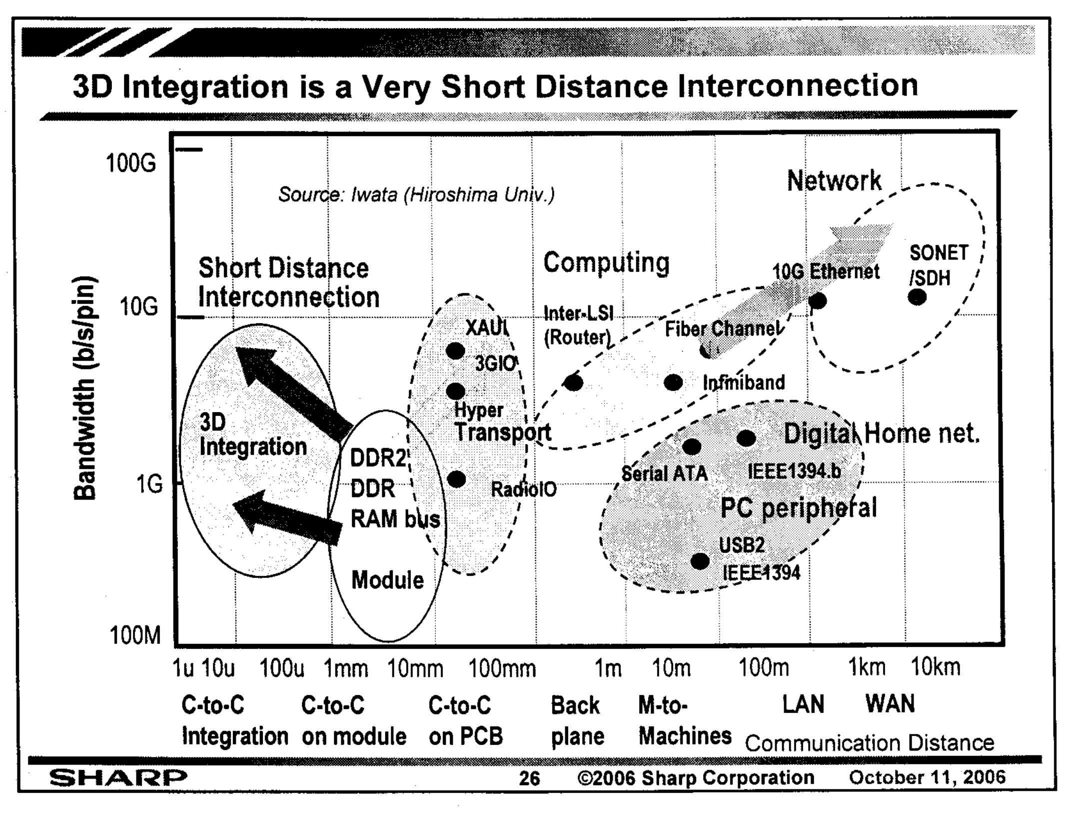
3D Integration is a Very Short Distance Interconnection
Source: Iwata (Hiroshima Univ.)
Bandwidth (b/s/pin)
100G
10G
1G
100M
Network
SONET /SDH
10G Ethernet
Computing
Inter-LSI (Router)
Fiber Channel
Infiniband
Short Distance Interconnection
3D Integration
DDR2 DDR RAM bus
Module
XAUI
3GIO
Hyper Transport
RadioIO
Serial ATA
IEEE1394.b
Digital Home net.
PC peripheral
USB2
IEEE1394
1u 10u 100u 1mm 10mm 100mm 1m 10m 100m 1km 10km
C-to-C Integration
C-to-C on module
C-to-C on PCB
Back plane
M-to-Machines
LAN
WAN
Communication Distance
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Characteristics of New Interconnect Technologies

	Interconnect Technology (Distance)	Data Rate	Power Consumption	Interconnect Density	Process	Cost	Chip Testing
Wire	Bonding Wire	X (2Gbps)	X	X	△	△	△
	Through Si Via	Iwata (Hiroshima University) ○ (8Gbps)	○	○	X	X	△
Wireless	Inductive Coupling	○ (10Gbps)	○	△	○	○	○

○ *Good*
△ *Fair*
X *Poor*

Source: Iwata (Hiroshima Univ.)

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Conclusion

1. **In the near future, these technologies will contribute new types of 3D-SiP.**
2. **However, whether TSV or some other technology will become dominant, and which technologies will be used in which applications depends on the results of R&D yet to come.**
3. **It is hoped that when these new technologies become the mainstream, they will produce 3D-SiPs that surpass SoC and usher in a new generation in the semiconductor industry.**

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